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RF Vacuum Microelectronics

based on Thin Film Edge-Emitter Technology

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We report the design, fabrication, and demonstration of thin-film-edge emitter vacuum diodes and transistors. The two-terminal device uses a thin-film-edge emitter as an electron source whose current density depends on the anode voltage. The three terminal device uses a thin-film-edge emitter as an electron source whose current density depends on the voltage applied to the extraction electrodes (gates). The emitted electrons are collected by the anode. All three electrodes (emitter, gate, and anode) are integrated on the same substrate. The devices have integrated on-chip resistors for burn-out prevention. The 3D microstructure was fabricated using IC and micromachining techniques. Contrasted with the usual vertical FEA structures, the particular vacuum transistor design invokes two dimensional vertical symmetry for the extraction electrodes (gate) using multi-layer thin film deposition techniques. The central thin-film-edge emitter is about 300 Å thick and is surrounded by two gate electrodes, one above and one below. The maximum radius of curvature using this approach is determined by the thickness of the deposited film. Emission currents as high as 50 μA / edge and current densities as high as 12.5 μA / μm and transconductances of 1.5 μS / μm have been demonstrated. The emission currents, in the absence of on-chip resistors, follow the Fowler-Nordheim relationship. This approach lends itself to low cost manufacturing and packaging because of the use of IC fabrication techniques and surface micromachining. The devices are quite attractive for providing high output power density at microwave frequencies at relatively low cost.

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Section 1. Program Overview

The objective of the RF Vacuum Microelectronics Amplifier Development program is to demonstrate a thin-film-edge emitter vacuum transistor (triode) technology for RF power sources with high-output-power density or high-specific power. The program is designed to meet the basic need for small, low cost, high-power-output density microwave amplifiers that can handle high power to fill the gap between low-efficiency, but reliable semiconductor devices and higher efficiency, but unreliable power tubes. Furthermore, semiconductor devices have lower manufacturing costs because of the batch fabrication techniques of IC manufacturing and micromachining. The RF vacuum microelectronics amplifier combines the small dimensions and batch fabrication advantages of semiconductor devices with the improved power handling capabilities of vacuum tubes.

Honeywell's technical approach to developing a high-power-density RF vacuum microelectronics amplifier is based on its unique thin-film-edge emitter vacuum transistor. The vacuum transistor utilizes a thin-film (200 - 400 Å) edge as an electron source. The thin-film-edge can be considered as an array of closely spaced field-emitting points, fabricated using conventional thin-film IC processing technology. Our analysis indicate the edge-emitter-based vacuum transistor has the greatest potential of all field emitter structures to achieve high transconductances and low input capacitances required for an RF source. This is possible because

- A thin-film-edge emitter vacuum transistor has small controlled radius of curvature leading to high current densities, transconductance, and efficiency.
- The gate electrodes have submicron dimensions and, thus, have low capacitance.
- Air-bridge interconnects lead to low parasitic capacitance.
- An integrated anode leads to low-cost fabrication, evaluation, and packaging.

The program was organized into three stages. In the first part of the program, a thin-film-edge vacuum diode was developed and demonstrated. In the second part of the program, a thin-film-edge vacuum transistor was designed, fabricated, and characterized. In the third part of the

program, the thin-film-edge vacuum transistor array was designed, fabricated, and characterized. The development path is illustrated in Figure 1.1, while the program schedule is shown in Figure 1.2.

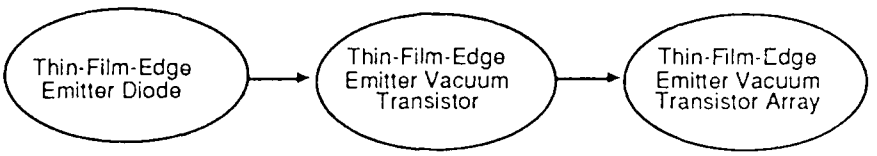


Figure 1.1. The thin-film-edge emitter vacuum transistor development path.

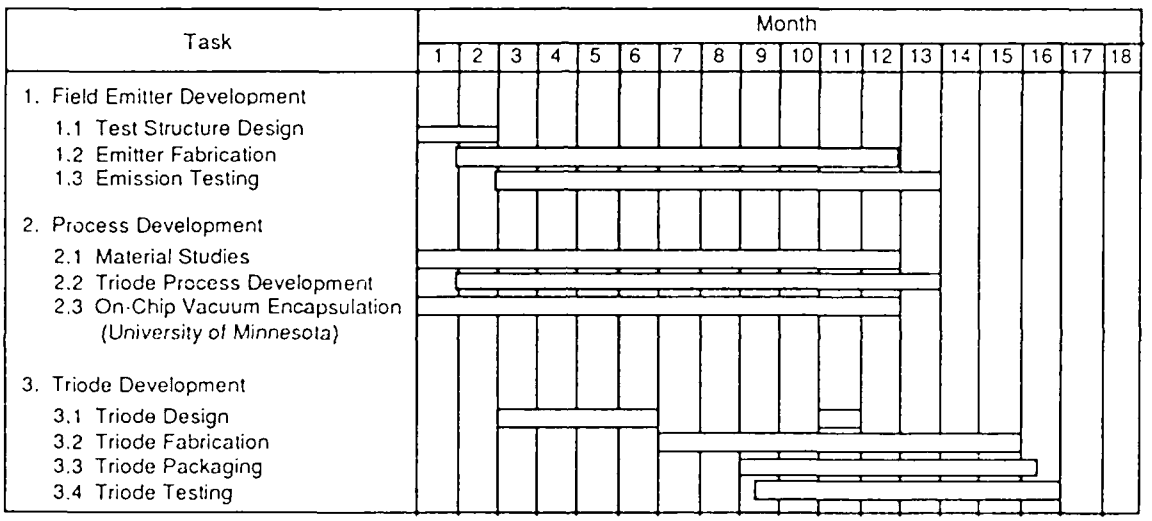


Figure 1.2. The RF Vacuum Microelectronics program schedule.

1.1 Program Objectives

The overall program objective was to demonstrate a vacuum triode with emission current density of 5 A/cm^2, a total current of 5 mA at a gate voltage less than 250 V that can be modulated at 1 GHz continuously for one hour. This was translated to a current density of 3 μA/μm for the edge emitter.

1.2 Program Accomplishments

The following are the accomplishments of the RF Vacuum Microelectronics Program

Vacuum Diode

- Demonstrated high emission current from a single edge ($\simeq$ 400 μA)
- Demonstrated high emission current density from an edge ($\simeq$ 10 μA/μm)
- Demonstrated high emission current from a comb structure with current equalization resistors without burnout
- Demonstrated long-term device operation (>72 hours) at a high current level (50 μA, 0.5 μA/μm)
- Performed a study of various emitter materials (TiW, WSi_x, Pt, WN_x, Mo)
- Demonstrated that the turn-on voltage can be reduced with Cs implants (from $\simeq$ 100 V to $\simeq$ 50 V)
- Demonstrated that Cs-implanted edge emitters can operate at high current densities (10 μA/μm). Operated a Cs-implanted edge emitter for ≥80 hours at 1 μA/μm.

Vacuum Transistor

- We have demonstrated a thin-film emitter vacuum transistor with symmetrically layered gate/control electrodes and integrated anodes
- The vacuum transistors have high currents (50 μA) and high current densities (10 μA/μm) and transconductance ≥1.5 μS. These values are above those considered necessary for 1 GHz operation.
- The devices have turn-on voltage as low as 50 V
- The devices have comb emitter structures with integrated resistors and capacitors on chip
- The devices have high-, short-, and long-range uniformity suggesting that large arrays of vacuum transistors can be connected in parallel to fabricate high-current and high-gain devices
- The devices have very low capacitances
- We have demonstrated all device and fabrication requirements necessary for 1 GHz operation of vacuum transistors with gain.

Process Development and Device Modeling

- Developed a thin-film resistor process with sheet resistances ranging from 1 Ω/sq to 10^7 Ω/sq for current equalization of vacuum transistors
- Developed silicon dioxide and silicon nitride processes for sacrificial layers and support layers resulting in mechanically robust vacuum transistors
- Developed processes for smooth thin-film-edge emitter that will result in smaller radius of curvature and higher currents and transconductance and higher frequency operation of the vacuum transistor
- Performed mechanical modeling and determined optimum vacuum transistor structure
- Performed electrostatic simulation for the determination of optimum emitter structure and the placement of the control electrodes. This resulted in a more robust vacuum transistor.
- Performed thermal modeling of the vacuum transistor to determine burnout mechanisms. This will have implications for future designs and post-fabrication processing.
- Performed a microwave analysis of the vacuum transistor to determine the optimum device parameters and device structure.

Modulation at 1 GHz

We did not demonstrate 1 GHz modulation even though the current density, transconductance, and capacitance of the vacuum transistor all indicate that modulation at 1 GHz should be possible. We attribute the lack of modulation to the following reasons:

- The total current obtained from the device was insufficient to drive our on-wafer probes used in our test system.
- The currents are not high because emission was not uniform. The area calculated from our analysis is only about 10^{-5} of the total potential emitting area for the wide devices.
- We believe that the emitting surface is covered with an oxide which can be removed using chemical cleans and in-situ hydrogen plasma clean. It should be possible to demonstrate 1 GHz modulation if these actions prove effective in removing the oxides.

Section 2. Field Emitter Array Amplifier

2.1 Field Emission Theory

The earliest proven theory of field emission or vacuum tunneling was developed by Fowler and Nordheim (Fowler and Nordheim, 1928). It described electron emission from a pure metal by a high electric field using a quantum mechanical tunneling mode to calculate the emission current density. According to Cutler, et al. (Cutler 1989), the field emission current is given by the product of the incident flux, transmission probability per electronic state, and occupation probability of the state.

For a 1-D barrier, the field emission current density is given by

$$J(F,T) = q \int_{Ea}^{\alpha} D(F,E)\, N(E,T)\, dE$$

where N(E,T) is the electron supply function, E is the normal kinetic energy in the tunneling direction, T is the absolute temperature; D(F,E) is the transmission coefficient or tunneling probability, q is the electronic charge, and Ea is the lowest energy of a tunneling electron.

$$N(E,T) = \frac{4\Pi m}{h^3}\left\{ \ln\left[1 + \exp\left(\frac{E - E_F}{kT}\right)\right]\right\}$$

where E_F is the Fermi energy. To determine the transmission, the solution to the Schrodinger equation is required, as was done by Fowler and Nordheim. Typically, this cannot be done in closed form, and it is necessary to resort to approximate methods to determine the transmission coefficient. Using the Wentzel-Kramers-Brillouin (WKB) approximation and assuming a potential barrier $V_{(x)}$

$$D_{WKB}(FE) = \exp\left\{-2\int_{x_1}^{x_2} K(x)\, dx\right\}$$

$$K(x) = \sqrt{\frac{2m}{h^2}(V(x) - E)}$$

x_1 and x_2 are the classical turning points where K(x) vanishes. For the Fowler-Nordheim model with an applied field, F, and no image interaction, V(x) is given by

$$V(x) = \Phi + E_F - qF(x)$$

where Φ is the work function and the classical image turning points are given by

$$x_1 = 0$$
$$x_2 = (\Phi + E_F - E)/qF$$

Using the WKB approximation

$$D_{WKB}(E) = \exp\left\{ \frac{-4qF}{3} \sqrt{\frac{2m}{h}} \left[\Phi - (E - E_F)\right]^{3/2} \right\}$$

Combining the expressions for N(E,T) and $D_{WKB}(E)$ in J

$$J = \frac{q^2}{8\Pi h\Phi} F^2 \exp(-2Q)$$

$$2Q = \frac{8\Pi\sqrt{2m}}{3qh} \frac{\phi^{3/2}}{F}$$

where J is the field emission current density, F is the electric field at the surface of the emitter, m is the electronic mass, q is the electronic charge, h is Plank's constant, and ϕ is the metal work function.

The current-voltage characteristics change very little in form when the image potential correction is applied. Without going through the derivation, the expression for current density in the presence of an image potential remains the same. However, the exponent is modified

$$2Q = \frac{8\Pi\sqrt{2m}}{3qh} \frac{\phi^{3/2}}{F} v(y)$$

where

$$y = \phi\sqrt{q^3F} = 3.79 \times 10^{-4} \frac{\sqrt{F}}{\phi}$$

ϕ is in Y and F is in V/cm.

The function V(y) can be approximated by [Spindt 1976]

$$v(y) = 0.95 - y^2$$

in the region of interest. The applied voltage is related to the field by $F = \beta V$, where β is the field factor and it is primarily dependent on the radius of curvature of the emitter. Assuming the emission area is α, Spindt, et. al. [Spindt 1976] showed that the emission current is given by

$$I = a_{FN} V^2 \exp\left[-\frac{b_{FN}}{v}\right]$$

where

$$a_{FN} = \frac{\alpha AB^2}{1.1\phi} \exp\left\{\frac{1.44 \times 10^{-7} B}{\sqrt{\phi}}\right\}$$

$$b_{FN} = \frac{0.95\, B\, \phi^{3/2}}{B}$$

$$A = 1.54 \times 10^{-6}$$

$$B = 6.87 \times 10^{7}$$

This is the expression for current density that is used in the design of devices.

2.2 Field Emitter Array Triode (Vacuum Transistor)

The drive to miniaturize the power booster has led to a renewed interest in vacuum microelectronic structures or field emitter arrays (FEAs). The FEA can be used to provide gated or modulated electron beams in power tubes (macro-devices), or can be used with in integrated anode as a triode or vacuum transistor (micro-device).

In both applications, the basic building block is the three-terminal FEA structure with a cold-cathode emitter as the electron source, a gate electrode for modulating the emitted electrons, and an anode for collecting the (emitted and modulated) electrons.

From the previous section, the anode (emitter) current is given by

$$I = a_{FN} V^2 \exp\left\{\frac{-b_{FN}}{V}\right\}$$

where all the parameters are defined in subsection 2.1.

The most important figure of merit for any device operating as an amplifier at high frequency is the unity gain cutoff frequency f_τ. It is given by

$$f_\tau = \frac{g_m}{2\Pi C}$$

where g_m is the device transconductance and C is the device capacitance.

To maximize f_τ, the transconductance must be increased while capacitance is decreased.

The transconductance of an FEA is given by

$$g_m = \frac{I}{V}\left[2 + \frac{b_{FN}}{V}\right]$$

To the first order

$$g_m = \frac{I}{V}\left[2 + \frac{0.95\,\beta\,\phi^{3/2}}{\beta V}\right]$$

β is the field factor and it is to the first order given by

$$\beta = \frac{1}{kr}$$

where k is between 5 and 15, and depends on the gate to emitter distance. Typically, 3×10^5 cm$^{-1} \leq \beta \leq 5 \times 10^5$ cm^{-1} in the operating regime.

The equivalent circuit of the gated field emitter is shown in Figure 2.2-1. The equivalent circuit shows the elements that determine the performance of the device. The most important are the gate capacitance and the transconductance. Another important element is the feedback capacitance between the gate and anode which determines the gain and f_{max}, but has no effect on f_τ.

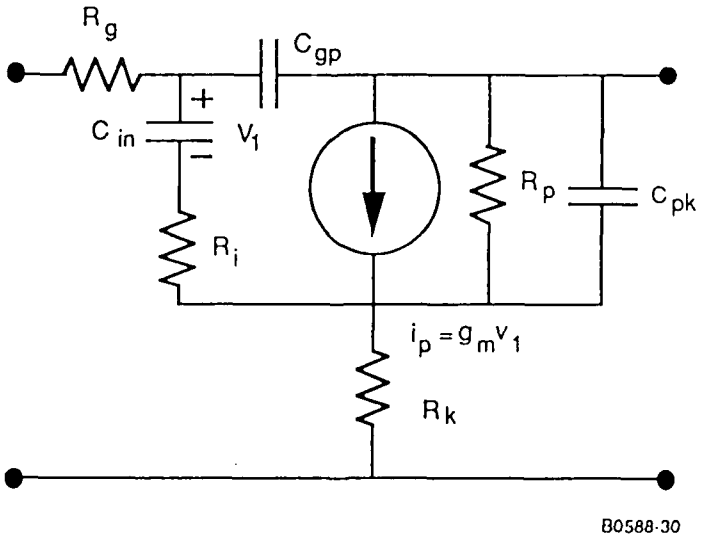


Figure 2.2-1. Simplified field emitter array triode equivalent circuit.

2.3 Thin-Film-Edge Vacuum Transistors

The drive to miniaturize the power booster has led to a renewed interest in vacuum microelectronic structures or field emitter arrays (FEAs). The FEA can be used to provide gated or modulated electron beams in power tubes (macro-devices). The most widely known vacuum microelectronic structure is the classical vertical "cone" FEA or Spindt cathode [Spindt, 1976; Gray, 1984], shown in Figure 2.3-1. It consists of a micro-size cell with a point-like vertical field emitter and an integrated circular aperture that surrounds the emitter tip. The FEAs were developed with the goal of replacing thermionic cathodes in TWT because of their higher current densities and longer lifetimes. They do not require heater power supplies and circuitry, as do thermionic cathodes, and they also avoid the problems of barium evaporation and other high-temperature-related problems. Furthermore, the emitted electrons are modulated. The ability to modulate electrons makes the vertical FEA ideal for injecting a pre-bunched electron beam into a helix TWT. The pre-bunched electrons are injected into a short beam tunnel, after which the beam passes through the gap of a klystron-like output cavity. The advantage of this approach is the significant reduction of the RF interaction length due to the injection of a pre-bunched electron beam. This leads to a reduction in size, an increase in power density, and an increase in total efficiency of the power booster relative to the miniaturized, conventional helix TWT.

A device based on this approach is, however, limited in three important areas. The first limitation is the length of the RF interaction region, which curbs device miniaturization. The structure is smaller than a conventional microwave tube, but it still has a relatively complex structure. The second is operating voltage. The high operating voltage needed to transport electrons through the long RF interaction region contributes to a very high power output, but also results in an expensive power supply. A large number of magnets are needed in a carefully aligned package to avoid spreading of the electron beam and collision with the slow wave structure. The third limitation is the cost. While this structure is smaller than a conventional traveling wave tube, it will be almost as costly. This will limit its application to situations where relatively high power output is a necessity.

Honeywell's technical approach to high-output-power-density RF amplifiers that overcome the limitations described above is the thin-film-edge emitter vacuum transistor, shown in Figure 2.3-1. It uses a lateral thin-film-edge emitter as electron source for an integrated vacuum transistor (micro-triode) with an on-chip anode. This approach to high-output-power-density RF amplifiers is directed at the much larger range of moderate-power applications that are sensitive to cost. It has the potential of meeting the program goal of high power density, microwave operation, and low manufacturing cost, with the potential to scale to higher power levels and high frequencies. For higher power levels and increased gain, the on-chip anode can be supplemented by off-chip anodes, but the basic configuration has the advantage of being extremely compact, lightweight, and low cost. Furthermore, compared to a point emitter structure, it can potentially handle much higher current densities per unit capacitance by distributing the emitting points along the edge and using a submicron gate, resulting in greater microwave gain for the simple triode structure. Compared to edge-emitter triodes using semiconductor materials, its current density capabilities are orders of magnitude greater. The number of free carriers in metals is on the order of $10^{23}/cm^3$, while in a semiconductor, they seldom reach $10^{20}/cm^3$. The thin-film-edge-emitter microwave vacuum transistor has the potential for low-cost manufacturing, because the device is fabricated using IC and micromachining techniques. Furthermore, the device has an integrated anode and does not require complex anode assembly techniques, resulting in inexpensive device screening and packaging. The next subsection describes this approach and its advantages in detail.

Thin-Film-Edge Emitter Vacuum Transistor

The thin-film-edge emitter vacuum transistor (MVT) is shown schematically in Figure 2.3-2. Figure 2.3-3 shows a cross section of the same device. It consists of a thin-film-edge emitter fabricated between two control electrodes (gates). The electrons emitted laterally from the thin-film edge is collected at the anode a few microns away.

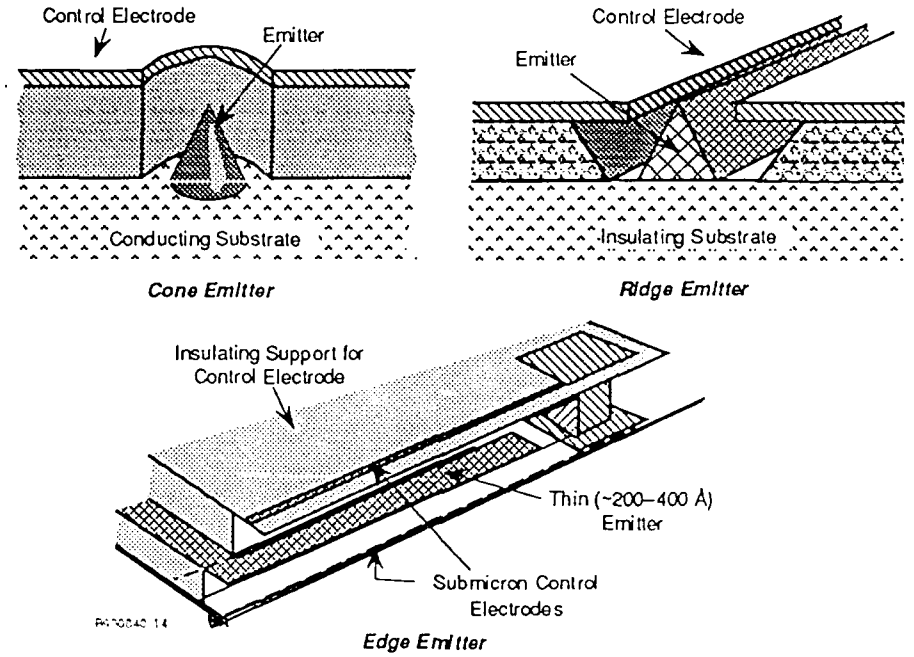


Figure 2.3-1. Classes of field emitter technology—cone emitter, ridge emitter, and edge emitter.

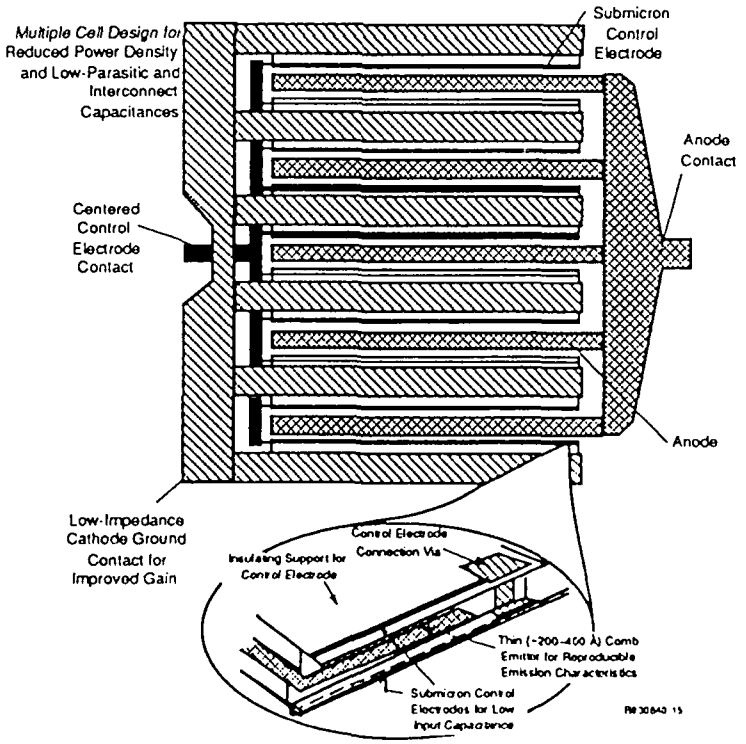


Figure 2.3-2. Thin-film-edge emitter vacuum transistor with low gate capacitance and high transconductance. The device can operate at high power output, high frequency, and high power density.

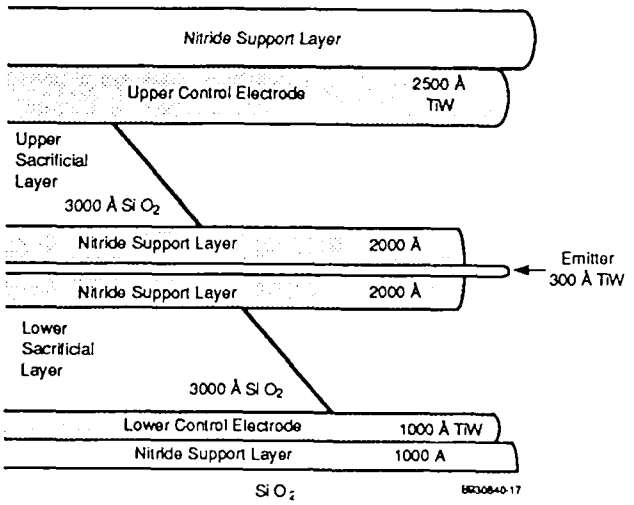


Figure 2.3-3. Cross section of the thin-film-edge vacuum transistor showing two-gate electrodes—one above and one below a 300 Å thick emitter. The separation between the emitter and the gate is 5,000 Å, and the gates have submicron dimensions for low capacitance.

The thin-film-edge emitter MVT invokes electrostatic potential symmetry with a symmetrically layered thin-film sandwich. A central thin-film-edge-emitter film is sandwiched between two extraction gate films, which lie above and below the emitter film (Figure 2.3-3). The edge of the emitter film becomes the electron source for the vacuum transistor. The advantages of this design are the following:

- The radius of curvature of the emitter is determined by the thickness of the thin film. It is less than or equal to half the thickness of the film. Film thicknesses are relatively easy to control by deposition processes.
- The spacing between the emitter and gate is also formed by controlled deposition processes.
- The thin-film-edge emitter is essentially a collection of closely spaced point emitters. Its principal advantage over the cone emitter is that it allows more emitter points (area) to be packed into the region between its gates than is possible with cone emitters, which are surrounded by gates.

- The capacitance between the submicron gate and the emitter is lower than the capacitance between the gate and emitter contact layer of a cone emitter.
- The device structure is flexible and can use a variety of emitter materials without the development of special processes for the deposition of new materials. For example, in the thin-film-edge emitter vacuum transistor, the emitter can be changed to use e-beam or sputter deposition, LaB_6, CeB_6 Cs-implanted W, or other low-work-function material.
- The anode is integrated on-chip, making device evaluation and packaging inexpensive compared to other approaches.
- The structure is inherently low cost, because it uses batch fabrication techniques developed for IC fabrication and micromachining.
- The anode is flexible in that it can be on-chip or off-chip. To use an off-chip anode, the on-chip anode is used as a focusing electrode by applying a modest negative bias.

2.4 TFEE Vacuum Transistor Development Path

Figure 2.4-1 summarizes our approach to the development of the thin-film-edge emitter vacuum transistor. The first phase was the development of the thin-film-edge emitter diode. This was followed by the development of the thin-film-edge emitter vacuum transistor. The final stage was the development of the thin-film-edge emitter vacuum transistor array which will be used in the implementation of a high-output-power microwave vacuum transistor.

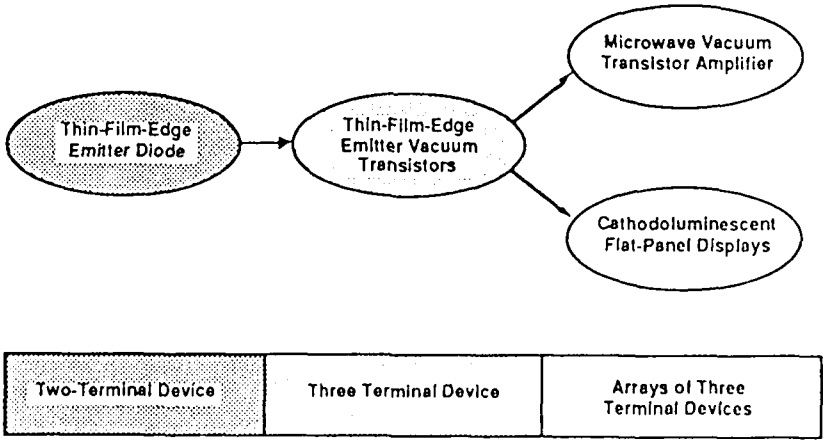


Figure 2.4-1. Development path of the thin-film-edge emitter vacuum transistor amplifier.

Section 3. Thin-Film-Edge Emitter (TFEE) Vacuum Diode

3.1 TFEE Vacuum Diode Design

The TFEE vacuum diode structure is shown in Figures 3.1-1 and 3.1-2. Figure 3.1-3 is a closer view of the vacuum gap region. The device has two terminals—emitter and anode. The anode is a thick layer of metal (usually 5,000 - 10,000Å) while the emitter is a very thin layer of metal (usually 200 - 400Å). The emitter is thin because a small radius of curvature is required for electron emission from the thin-film-edge. The radius of curvature of the emitter is less than or equal to half of the thickness of the emitter. As discussed in Section 2, the radius of curvature (and, hence, the emitter thickness) determines the electric field at the emitting edge. The electric field F is related to the applied voltage V through

$$F = \beta V$$

where B is the field factor and it is given by

$$\beta = \beta(r,d) = \frac{1}{2\, r \ln\left(\frac{d}{r}\right)}$$

where r is the radius of curvature and d is the anode-emitter separation. In most cases, B is approximated by

$$\beta \approx \frac{1}{kr}$$

where $5 < k < 15$.

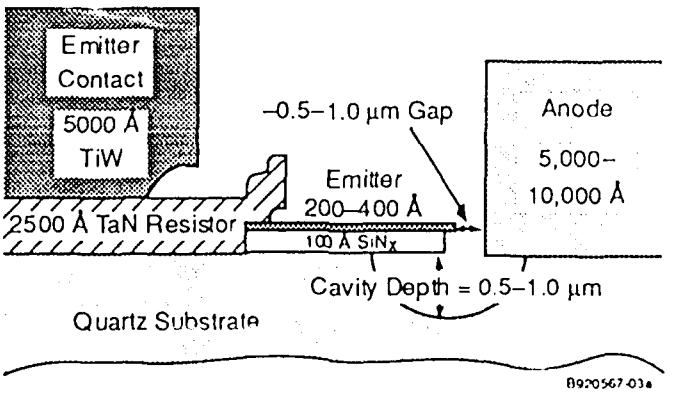
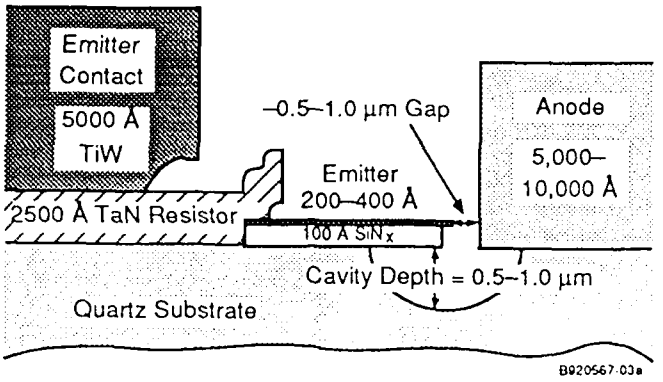
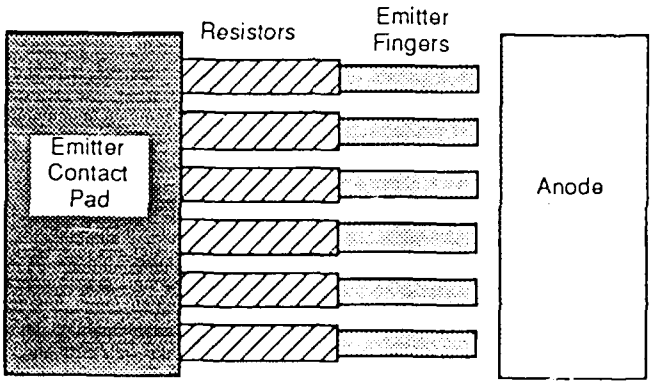


Figure 3.1-1. Thin-film-edge emitter vacuum diode structure—side view.



Side View



Top View

Figure 3.1-2. Thin-film-edge emitter vacuum diode structure—top view.

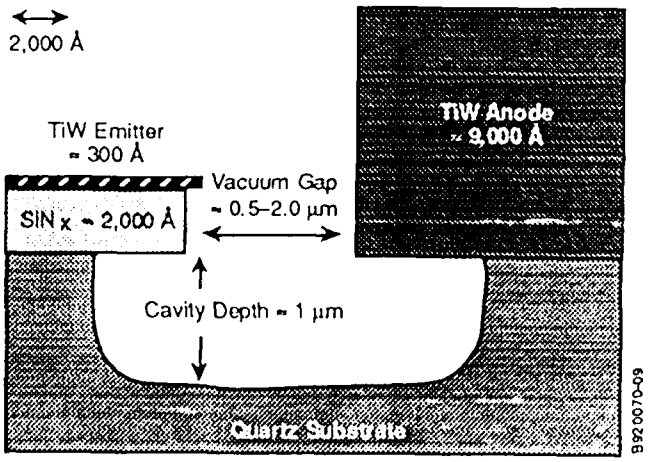


Figure 3.1-3. Thin-film-edge emitter vacuum diode structure—closer view of gap.

There were four types of devices designed. These are (I) solid emitters with varying widths, (II) solid emitters with series resistors and varying widths, (III) comb emitters, and (IV) comb emitters with a series resistor for each emitter finger.

Solid/Continous Emitters

The emitter widths of the diodes was varied from 2 μm to 100 μm, while the gap was varied from 0.25 μm to 1 μm.

Solid/Continous Emitters with Resistors

The emitter widths of the diodes was varied from 2 μm to 100 μm, while the gap was varied from 0.25 μm to 1 μm. The resistors are in series with the emitter.

Comb Emitters

There are two comb emitter finger widths. The first has 2.5-μm-wide fingers with 2.5 μm spacings while the second has 5-μm-wide fingers with 5 μm spacings. The devices have the following number of emitter fingers: 2, 4, 6, 8, 12, and 16.

Comb Emitters with Resistors

The width and number of emitters is same as above. Each emitter finger has a series resistor. In some cases, the resistor is not segmented as the fingers.

A complete mask documentation (5316) has been delivered to ARPA and its representatives.

3.2 TFEE Vacuum Diode Fabrication

The fabrication process outline is given in Appendix A. The fabrication starts with a quartz wafer or a Si wafer with 5 μm of oxide. A layer of nitride is deposited by reactive sputtering followed by the thin emitter layer. This is followed by lithography and plasma etch of the emitter and nitride layers. An oxide layer is next deposited, and this is patterned to define via holes for contact between the resistor layer and the emitter layer. The resistor layer is TaN. It is next deposited by reactive sputtering, and it is defined by plasma etch with the oxide acting as an etch stop. Another layer of oxide is deposited and via holes defined. A thick layer of metal is next

sputter deposited. This metal layer is the anode as well as the emitter contact. It is defined by plasma etch with oxide acting as an etch stop.

The final setup in the fabrication is the sacrificial layer etch to define the vacuum gap. This is done in BOE. Figures 3.2-1 and 3.2-2 are SEMs of completed vacuum diodes.

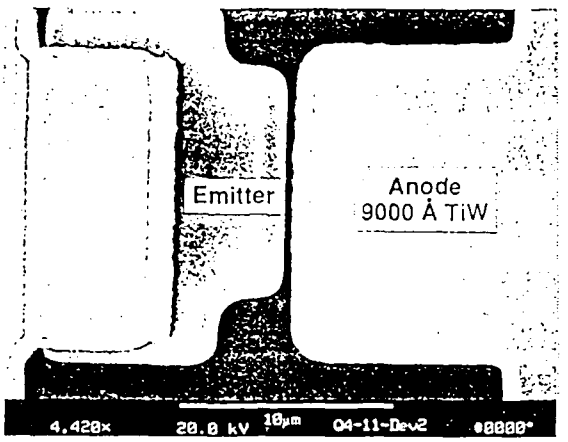


Figure 3.2-1. Scanning electron micrograph of the vacuum diode.

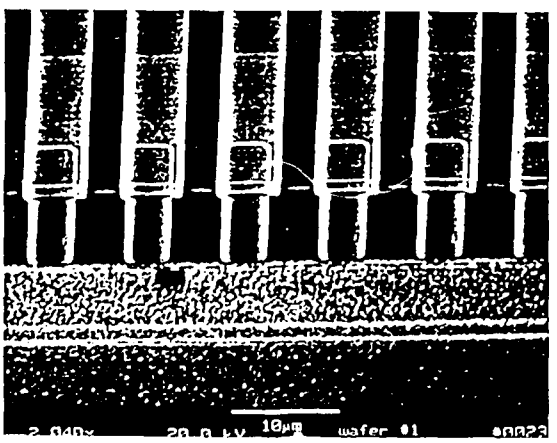


Figure 3.2-2. Scanning electron micrograph of the vacuum diode showing the emitter fingers.

3.3 Vacuum Diode Characterization and Evaluation

The test system for the characterization of the TFEE vacuum diode is shown in Figure 3.3-1. It is an ultra high vacuum system with typical base pressures <1 x 10^{-9} torr. It has two Keithley 237 source measure units capable of measuring or sourcing a current of 1 fA or a voltage of 1000

V. The wafers can be baked in UHV up to 500°C. The test setup for the vacuum diode is shown in Figure 3.3-2. The anode is biased with a Keithley 237 SMU while the emitter current is monitored by a Keithley 617 multimeter.

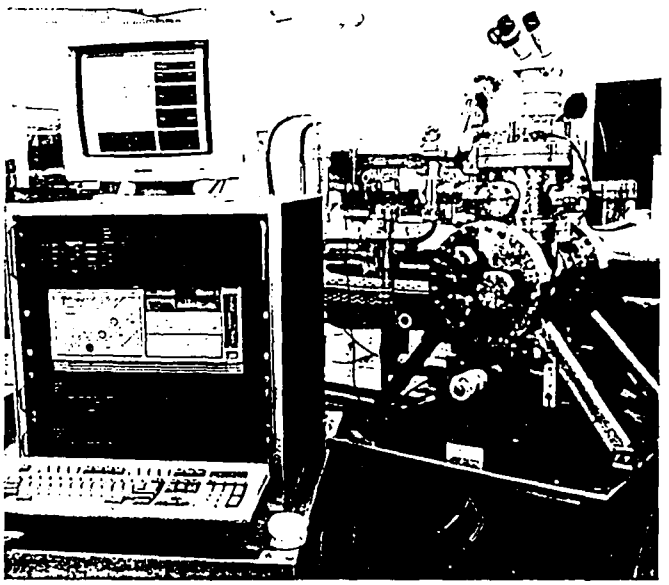


Figure 3.3-1. Vacuum test chamber.

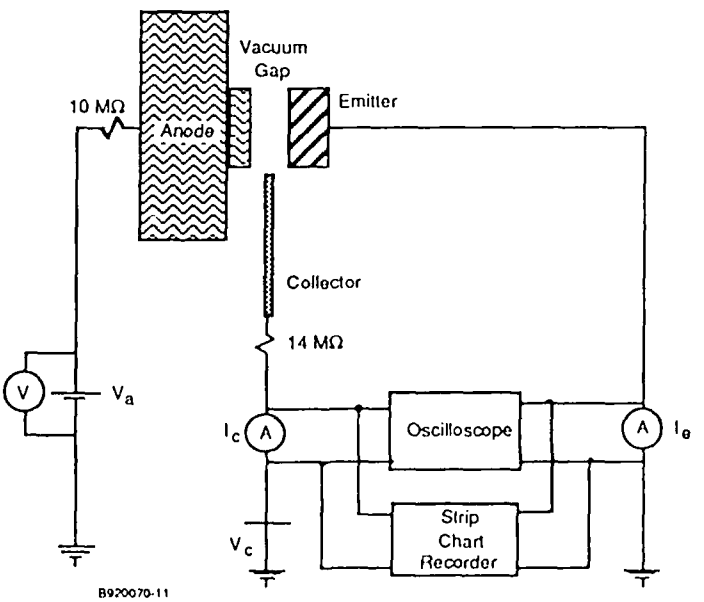


Figure 3.3-2. Vacuum diode test setup.

This report will only give a summary of the device results obtained.

Solid Emitters

Figure 3.3-3 is an IV characteristics of a 100- μm-wide diode. The emitter is 300Å TiW. The anode-emitter distance is 0.5 μm while the vacuum cavity is about 1 μm deep. The wafer was baked out in vacuum at 250°C prior to the measurements. The figure shows that a current of 400 μA was obtained from a single edge. This is the highest current ever obtained from a single edge. Figure 3.3-4 shows the Fowler-Nordheim plot for the TiW edge. An analysis of the data shows that the Fowler-Nordheim constants are given by

$$a_{FN} = 1.854 \times 10^{-6}$$

$$b_{FN} = 1041.2$$

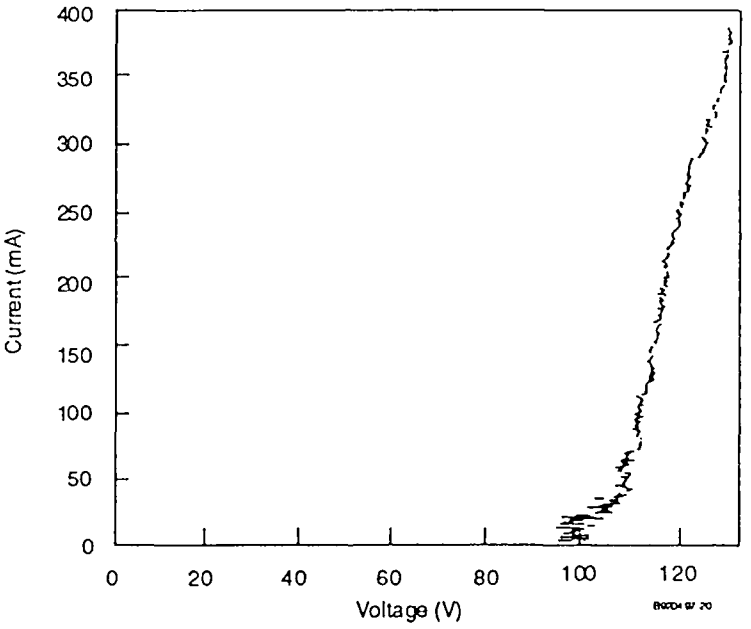


Figure 3.3-3. IV characteristics of a 100-μm wide vacuum diode.

We can deduce the emitting area from the values of a_{FN} and b_{FN} if we assume a value for the emitter work function. If the work function is varied between 3.5 eV and 5.5 eV, the emitting area α does not vary by much; however, the field factor varies by almost a factor of two. The result is displayed in Table 3.1.

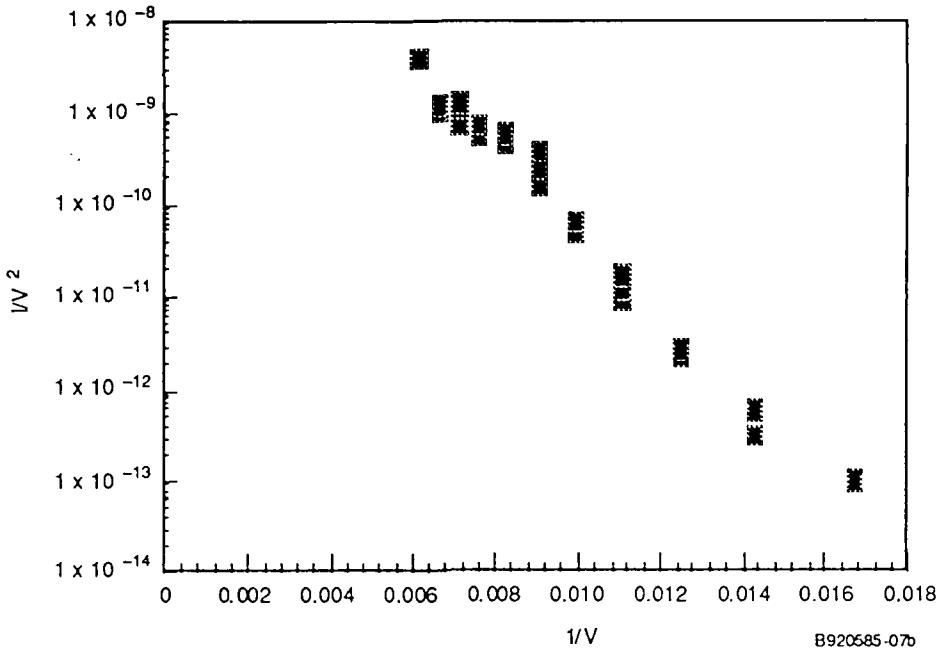


Figure 3.3-4. Fowler-Nordheim characteristics of a 100-μm wide vacuum diode.

Table 3.1. Summary of TiW Emitters.

Device Width	Maximum Current	Current Density
5 μm	48 μA	9.6 μA/μm
10 μm	59 μA	5.9 μA/μm
20 μm	165 μA	8.25 μA/μm
50 μm	288 μA	5.75 μA/μm
100 μm	383 μA	3.8 μA/μm

The table shows that the emitting area does not change significantly with the change in the work function. If we assume the work function is 4.5, the field factor β is $\simeq$ 5.98 E5 cm^{-1}, while the emitting area $\alpha = 1.57 \times 10^{-13}$ $cm^2 = 1.57 \times 10^3$ $Å^2$.

The nominal emitting area is 0.25 πrl, where r is the radius of curvature and l is the emitter width. We made assumption that electron emission occurs only over $\pi/4$ angle. For a 300Å film with 100 μm length, the nominal emission area A_E is 1.18×10^{-8} cm. The total emitter surface is much more than the area calculated. If we assume that $\beta = 1/kr$ with $k \simeq 10$, then theoretical

value of $\beta = 6.67 \times 10^4\ cm^{-1}$, we immediately observe that experimental value of β is much higher than the theoretical value. If we use the experimentally derived β to calculate the radius of curvature of emitting surface, we obtain $r_B = 1.672 \times 10^{-7}$ cm or 16.7Å. We can calculate the equivalent emission area with this radius of curvature $A_{eq} = \pi r_B^2 = 8.79 \times 10^{-14}$ which is only a factor of 2 from α, suggesting that electron emission is only taking place from one or two emission sites on the emitter surface. This radius of curvature r_β is very small compared with what is expected from a 300 Å thick film. The radius of curvature calculated from β is a factor 10 lower than the expected radius of curvature.

We can speculate that electron emission is coming from a small burr on the surface of the emitter. If we assume that the emission angle is 1/4 of that of a sphere, then the emission area $\alpha_c = \pi r_\beta^2 = 8.79 \times 10^{-14}$. The emission area calculated for a small burr on the surface is not too different from the emission area $\alpha = 1.57 \times 10^{-13}\ cm^2$ derived from the Fowler-Nordheim analysis of the data. The calculated emission area α_c and the derived emission area α is consistent with the idea that a single grain on the surface is contributing to electron emission.

The data and analysis suggests the electron emission is from a small area on the surface of the emitter. It also suggests the emitter is not smooth and emission is dominated by grains or grain size. Finally, the emitter surface (and emission sites) is probably covered with an oxide leading to most sites not emitting, and emission is only occurring on a few sites not covered with an oxide.

Comb Emitters with Resistors

Figure 3.3-5 shows SEM of the comb emitter vacuum diode, while Figure 3.3-6 shows a closer view of the same device. The emitter fingers are 5 μm and are separated by 5 μm spaces. Figure 3.3-7 is an IV characteristic of the comb emitter vacuum diode with series resistors. The data was taken first in the forward direction with device turning on at about 100 V. Then, the polarity was reversed. We observe that the current is insignificant even at -300 V. The measurements in the forward direction was repeated. The forward IV characteristics was duplicated. The emitter has four fingers and each emitter has a series resistance of 5 MΩ.

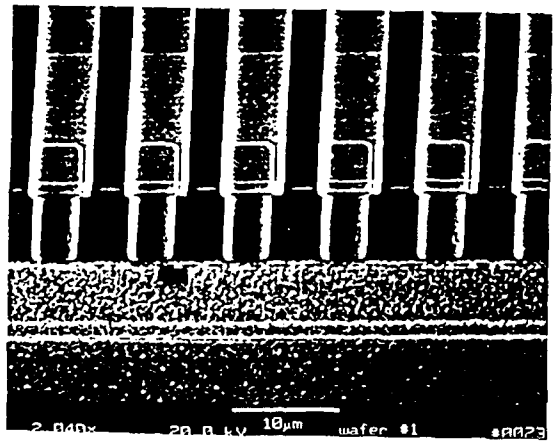


Figure 3.3-5. SEM of vacuum diode with comb emitters and integrated resistor.

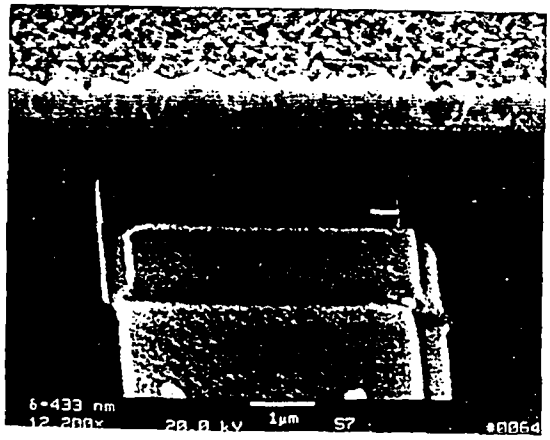


Figure 3.3-6. SEM of vacuum diode with comb emitters and integrated resistor—closer view.

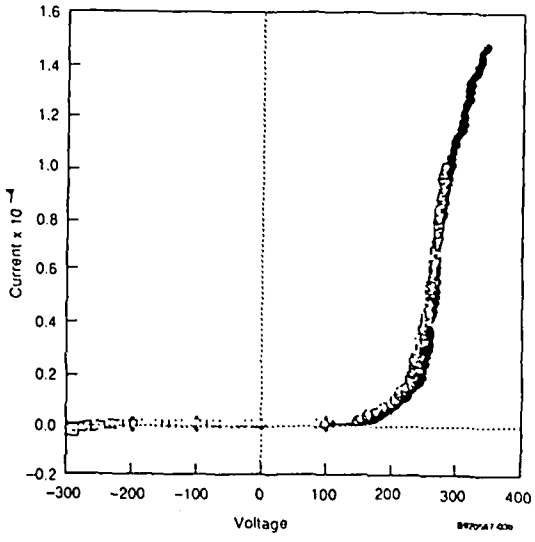


Figure 3.3-7. IV characteristics of a vacuum diode (in forward and reverse directions) with comb emitters and integrated resistors.

Summary of Emitter Results

We measured the maximum emission current as a function of emitter width. The results presented in Table 3.2 show that the emission current density seems to decrease with emission width. The data is consistent with the idea that there is a distribution of emitter sites of which only a handful are clean and are then responsible for the electron emission. The probability of finding such a site increases with the length of the emitter. If the emission sites are cleaned by wet chemistry or a plasma, we expect the emission current to be more uniform.

Table 3.2. Summary of Emitter Materials.

Emitter Material	Max Current	Max Current Density
TiW	380 μA	9.6 μA/μm
Pt	6 μA	0.6 μA/μm
Mo	10 μA	1 μA/μm
WSix	250 μA	7.8 μA/μm
WNx	118 μA	9.1 μA/μm

We also measured the maximum emission current and maximum current density as a function of emitter material. Table 3.3 shows that there is a strong dependence of maximum emission current density on the emitter material. The best materials in terms of maximum current density contained W, a refractory metal.

Figure 3.3-8 shows the long-term test of a continuous emitter that was stressed at current of 50 μA for 4000 mins. The voltage drifted very little from 130 V that was applied. The emitter width is 100 μm with a current density of 0.5 μA/μm.

Performance Improvement with Cs Implant

The key to improving the performance of thin-film-edge emitter vacuum diode is the reduction of the factor b_{FN} in the modified FN equation

$$b_{FN} = \frac{6.53 \times 10^7 \phi^{3/2}}{\beta}$$

b_{FN} is reduced if β increases and ϕ decreases. We carried out experiments to reduce the work function by introducing an alkali into the emitter. We implanted Cs at 120 keV into a 300 Å TiW film with a dose of 2E15 cm^{-2}. The implant profile was chosen such that Cs profile peak was at the center of the edge. The implant profile parameters were Rp = 148Å and ΔRp = 98Å.

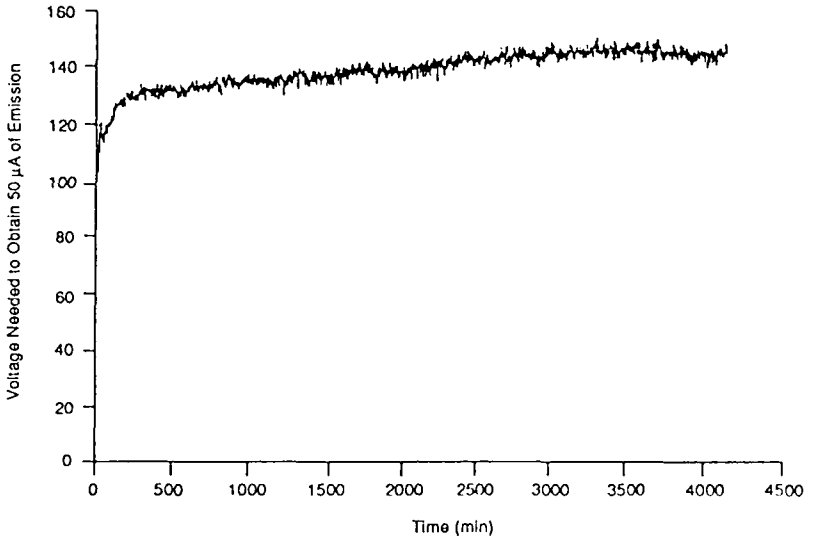
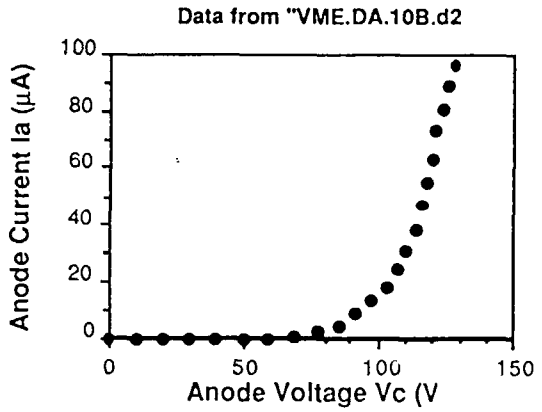


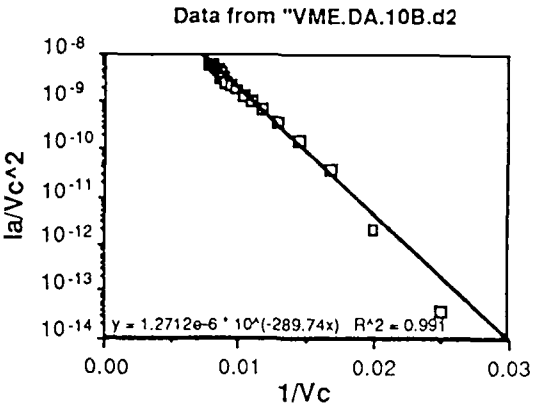
Figure 3.3-8. Long-term test of a 100-µm wide continuous edge emitter biased at 0.5 µA/µm.

Figure 3.3-9 is the IV characteristics of a vacuum diode with Cs implant. Also shown is the corresponding FN plot. Figure 3.3-10 is the IV characteristics of a similar vacuum diode without Cs implant. Also shown is the corresponding FN plot.

Our analysis of the FN plot for the Cs-implanted sample shows that $a_{FN} = 1.27 \times 10^{-6}$ A and $b_{FN} = 667.2$. The corresponding numbers for un-implanted wafer are $a_{FN} = 1.08 \times 10^{-6}$ A and $b_{FN} = 1438.8$.

We can conclude that the devices have similar emission areas since a_{FN} are about equal, while there is a factor 2 difference in b_{FN}. The change in b_{FN} can be attributed to a reduction in work function if we make the assumption that the field factor is the same. However, this is only a speculation.





IV Characteristic:

$I \geq 10\ \mu A/\mu m$

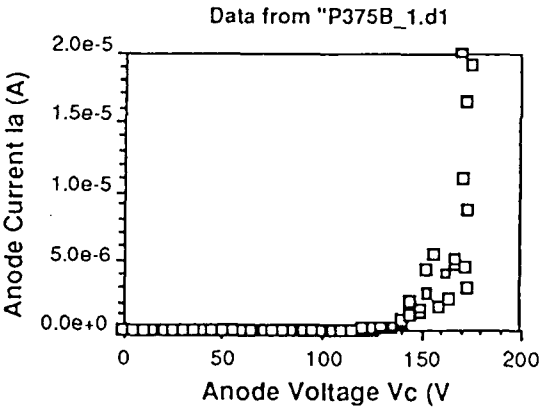
$W = 10\ \mu m$

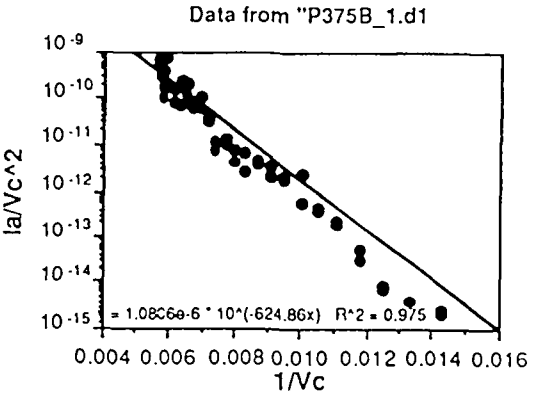
Fowler-Nordheim Pl

$a_{FN} = 1.271 \times 10^{-6}$

$b_{FN} = 667.2$

Figure 3.3-9. IV characteristics and FN plot of a 10-μm wide TiW emitter implanted with Cs.





IV Characteristic:

$I \simeq 4\ \mu m/\mu m$

$W = 5\ \mu m$

Fowler Nordheim Pl

$a_{FN} = 1.08 \times 10^{-6}$

$b_{FN} = 1438.$

Figure 3.3-10. IV characteristics and FN plot of a 5-μm wide TiW emitter.

Figure 3.3-11 is a long-time test of a Cs-implanted wafer biased at a current of 1 μA/μm. The device ran for 80 hours before the test was stopped. It shows that the current of 1 μA/μm (20 μm) was sustained at about 110 V for most of the time after which the voltage increased at 140 V.

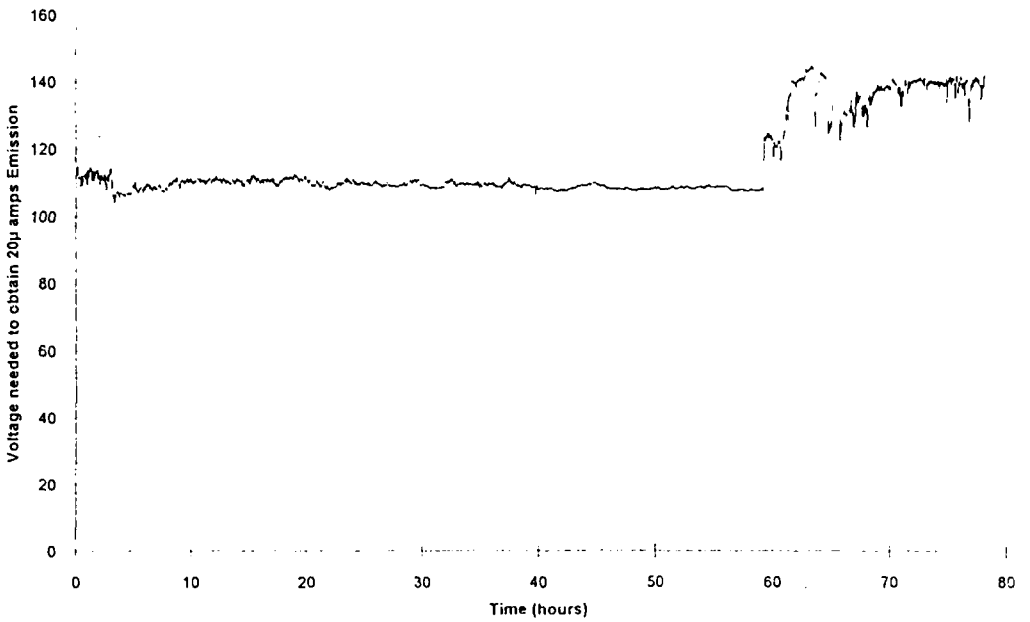


Figure 3.3-11. Long-term emission test for Cs-implanted TiW emitter.

The data shows that Cs-implanted thin-film-edge emitter vacuum diodes are stable and in contrast to surfaces treated with Cs.

Summary of Vacuum Diode Results

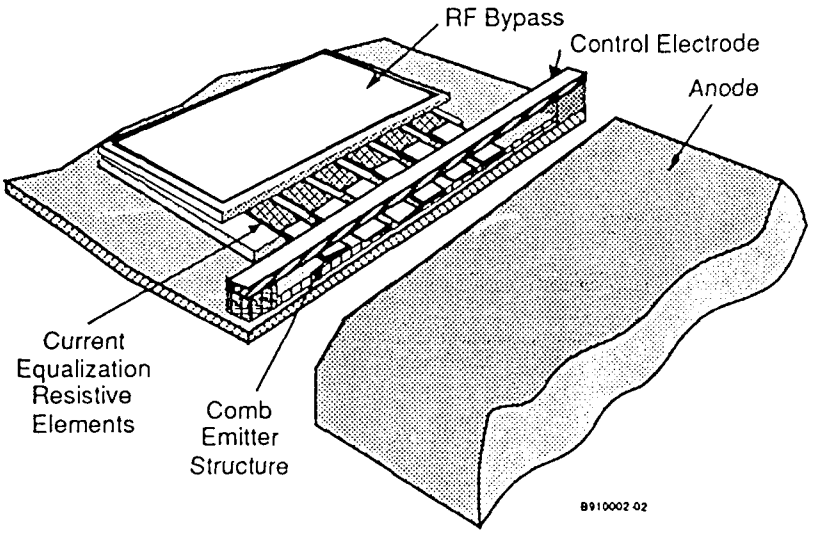
We demonstrated the thin-film-edge emitter concept, and we studied various emitter materials. We found out that W and W-containing alloys or compounds have the highest current carrying capabilities. We demonstrated high emission current ($\simeq$ 400 μA) from a single edge, and we also demonstrated the highest emission current density ($\simeq$ 10 μA/μm) to date. We demonstrated high emission currents without burnout using a comb emitter structure and current equalization resistors. We showed that devices can be operated at 1 μA/μm current density over a long period (>72 hours). We demonstrated that Cs implantation can be used to reduce the turn-on voltage and the resulting devices are capable of operating at high current densities (10 μA/μm) and over long period of time at moderate stresses (1 μA/μm for >80 hours). The results indicate that the thin-film-edge emitter can be used as an electron source for a vacuum transistor.

Section 4. Thin-Film-Edge Emitter Vacuum Transistor

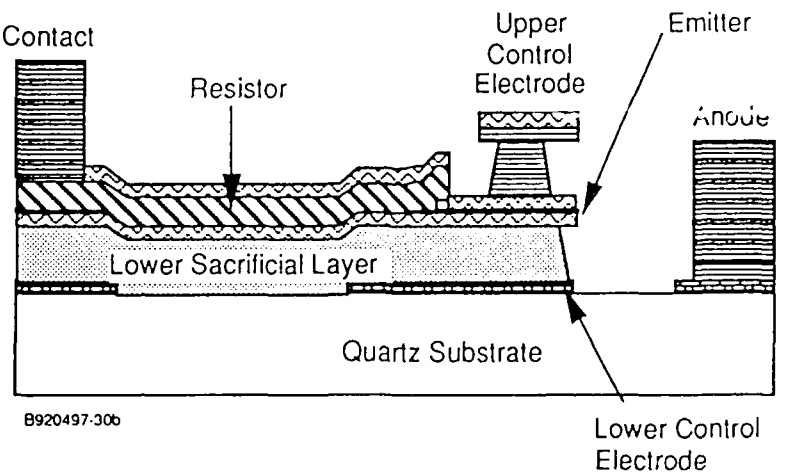
The thin-film-edge emitter vacuum transistor, shown in Figure 4.1, consists of a thin-film-edge emitter incorporated between two control electrodes (gates). The electrons emitted laterally from the thin-film-edge is collected at the anode a few microns away. The thin-film-edge emitter vacuum transistor invokes electrostatic potential symmetry with symmetrically layered thin-film sandwich. A central thin-film-edge emitter film is sandwiched between two extraction gate films which lie above and below the emitter film as shown in Figure 4.2. The edge of the emitter film becomes the electron source for the vacuum transistor. The advantages of this design are the following (i) the radius of curvature of the emitter is determined by the thickness of the thin-film. It is less than or equal to half the thickness of the film. Film thicknesses are relatively easy to control by deposition processes. (ii) the spacing between the emitter and gate is also formed by controlled deposition processes. (iii) the thin-edge emitter, in essence, is a collection of closely spaced point emitters. Its principal advantage over the cone emitter is that it allows more emitter points (area) to be packed into the region between its gates than is possible with cone emitters which are surrounded by gates. (iv) the capacitance between the submicron gate and the emitter is lower than the capacitance between the gate and emitter contact layer of a cone emitter. (v) the device structure is flexible and can use a variety of emitter materials without the development of special processes for the deposition of new materials. For example, in the thin-film-edge emitter vacuum transistor, the emitter can be changed to use e-beam or sputter deposition, LaB_6, CeB_6, Cs-implanted W, or other low work function material. (vi) the anode is integrated on-chip making device evaluation and packaging inexpensive compared to other approaches. (vii) the structure is inherently low-cost because it uses batch fabrication techniques developed for IC fabrication and micromachining. (viii) the anode is flexible in that it can be on-chip or off-chip. To use an off-chip anode, the on-chip anode is used as a focusing electrode by applying a modest negative bias.

Device Design

The device shown in Figure 4.1 and 4.2 is based on gated electron emission from a thin-film-edge. The emission current from a thin-film-edge is given by the Fowler-Nordheim equation shown below.



Conceptual View of Vacuum Transistor



Side View of Vacuum Transistor

Figure 4.1. Thin-Film-Edge Emitter Vacuum Transistor with Low Gate Capacitance and High Transconductance.

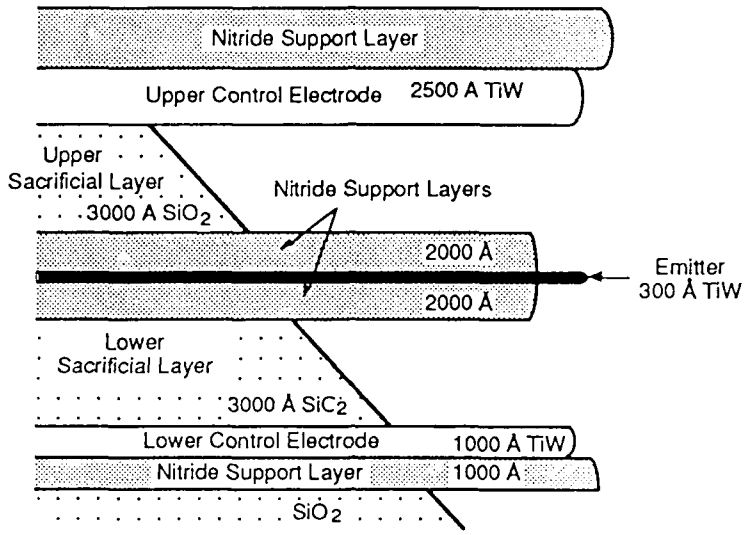


Figure 4.2. Cross-Section of the Thin-Film-Edge Emitter Vacuum Transistor Showing Two Gate Electrodes—One Above and One Below a 300 Å-thick Emitter. The separation between the emitter and gate is 5,000 Å, and the gates have sub-micron dimensions for capacitance.

Current Density and Transconductance

The principal device performance parameter are the current density and device transconductance. They are dependent on (i) the radius of curvature of the emitter, and (ii) the work function.

The current density is given by

$$I = a\, V^2 \exp\left[-\frac{b}{V}\right]$$

$$g_m = \frac{I}{V}\left[2 + \frac{b}{V}\right]$$

where

$$a = \alpha \frac{A\beta^2}{1.1\,\phi} \exp\left[\frac{1.44 \times 10^{-7} B}{\sqrt{\phi}}\right]$$

$$b = \frac{0{\cdot}95\, B\, \phi^{3/2}}{\beta}$$

$A = 1{\cdot}54 \times 10^{-6}$

$B = 6{\cdot}87 \times 10^{7}$

α = emission area.

$\emptyset$ is the work function, V is the applied voltage, and β is the field factor and it gives the relationship between the electrostatic field, E, at the emitting edge and the applied voltage ($E = \beta V$).

To the first order ,

$$g_m = \frac{I}{V}\left[2 + \frac{0.95\ B\ \emptyset^{3/2}}{\beta V}\right]$$

The most important structural parameter is β, the field factor. Typically, $\beta \approx 2 - 5 \times 10^5$ and β is 1/kr where r = radius of curvature, k is between 5 and 15, and depends on distance of gate to the emitter.

It is, therefore, very important to understand the dependence of the electrical field at the emitter tip on the applied voltage, the radius of curvature, and the device dimensions. This must be balanced with the need to maintain structural integrity of the microstructure during fabrication, when forces due to surface tension are in effect, and during device operation, when there are electrostatic forces between the electrodes. We performed a simulation of the 3D microstructure using ANSYS to determine the nominal electrostatic field at the emitter tip assuming that it is perfectly smooth. Figure 4.3 is the device structure that was simulated. Figure 4.4 shows the electrostatic field contours around an emitting edge that is 300 Å thick. It shows that if the emitter is perfectly smooth (which it is not), the electrostatic field at the emitter is greater than 1×10^7 V/cm. Nominally, an electrostatic field of 4×10^7 V/cm will be required to obtain any appreciable emission from the edge. However, since the edge is a thin-film, we expect that there will be a distribution of the grain sizes leading to much smaller radii of curvature than the thickness and, hence, much higher electrostatic fields. We also studied the effect of the placement of the upper gate relative to the emitter while keeping the lower gate self-aligned to the emitter. The simulations indicate that the maximum electric field will vary by about 3% from the nominal value if the gate is misaligned by 0.2 μm, while a misalignment of 0.5 μm will lead to variations as large as 15%. This is rather serious since the emission current depends

exponentially on the maximum electric field. This can be mitigated by using self-aligned techniques of defining the emitter edge.

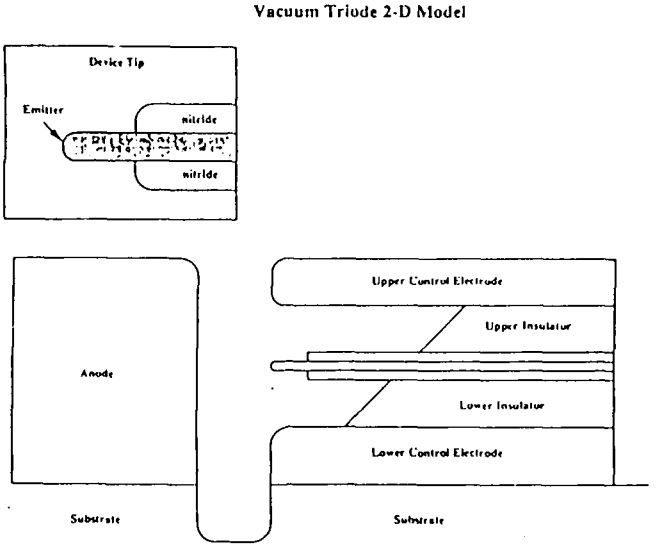


Figure 4.3. Device Structure Simulated using ANSYS.

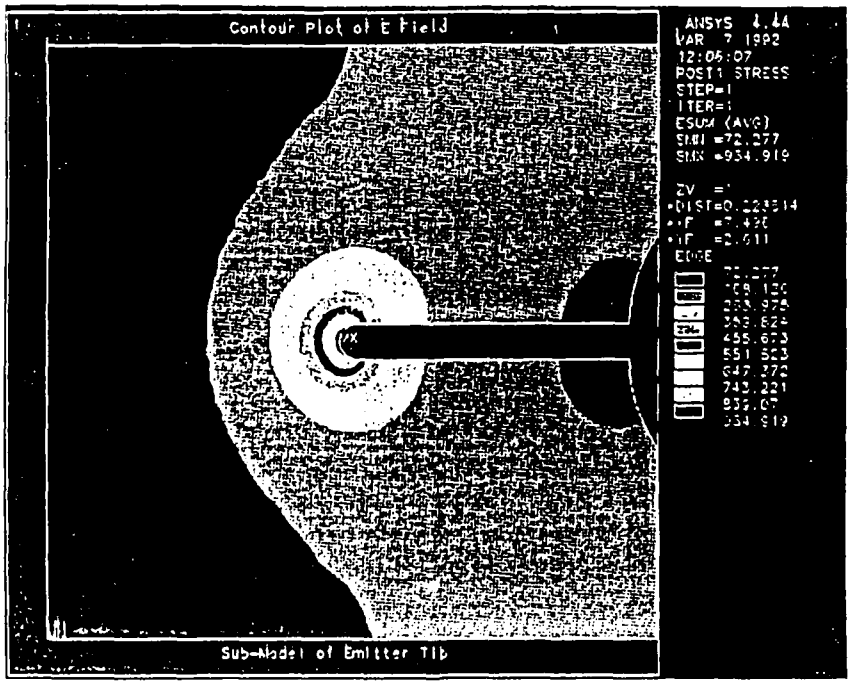


Figure 4.4. Electrostatic Field Contours of 300 Å Thick Emitters. The gate/emitter separation is 5,000 Å and the anode/emitter separation is 5 μm. The maximum electric field is 1 x 10^7 V/cm. The gate voltage is 100 V while the anode voltage is 400 V.

We also performed electro-mechanical simulation of the structure using ANSYS. With 300 V applied to the gate, the emitter only deflected 150 Å, while the upper gate deflected less than 40 Å. Our simulations included the intrinsic stresses of deposited films. The deflections were insensitive to small changes in the sacrificial oxide layer thickness and small changes in the nitride thickness, but it was very sensitive to the intrinsic stresses of the deposited films.

Finally, we examined the thermal effects of using high voltages and currents on each electrode. If we assume an anode voltage of 500 V and an electron current density of 10 μA/μm of edge width, we found that the emitter temperature rise from ohmic heating is insignificant. Similarly, the anode temperature rise from electron bombardment is insignificant. However, if we assume a gas particle is desorbed and ionized, the ionized particles go to the emitter. The temperature rise of the emitter from ionized particle bombardment is > 3400 °C, and it is strongly dependent on the emitter layer thermal conductivity.

The design and fabrication issues that needed to be balanced were (i) electrostatic deflection of the electrodes, (ii) oxide and nitride breakdown, (iii) device turn-on voltage, (iv) thermal effects at the anode, and (v) evolution of adsorbed gasses from the thin films. Based on these considerations, we designed the device to the structural specifications shown in Table 4.1.

Table 4.1. The design parameters for the vacuum transistor based on above mentioned design and fabrication considerations.

Device Parameter	Value
Emitter Thickness	300 Å
Gate / Emitter Separation	5000 Å / 7000 Å
Anode / Emitter Separation	5 μm
Gate Width	4 μm
Emitter, Anode, Gate Material	TiW

Device Fabrication

The device shown in Figures 4.1 and 4.2 is a 3D microstructure that is fabricated using IC processing and micromachining techniques. The fabrication process flow is shown in Figure 4.5. The process consists of nine masking steps because of the addition of a resistor layer. Without a resistor layer, the fabrication process has seven masking steps and one more mask can be eliminated if the emitter edge is defined by a self-aligned cut.

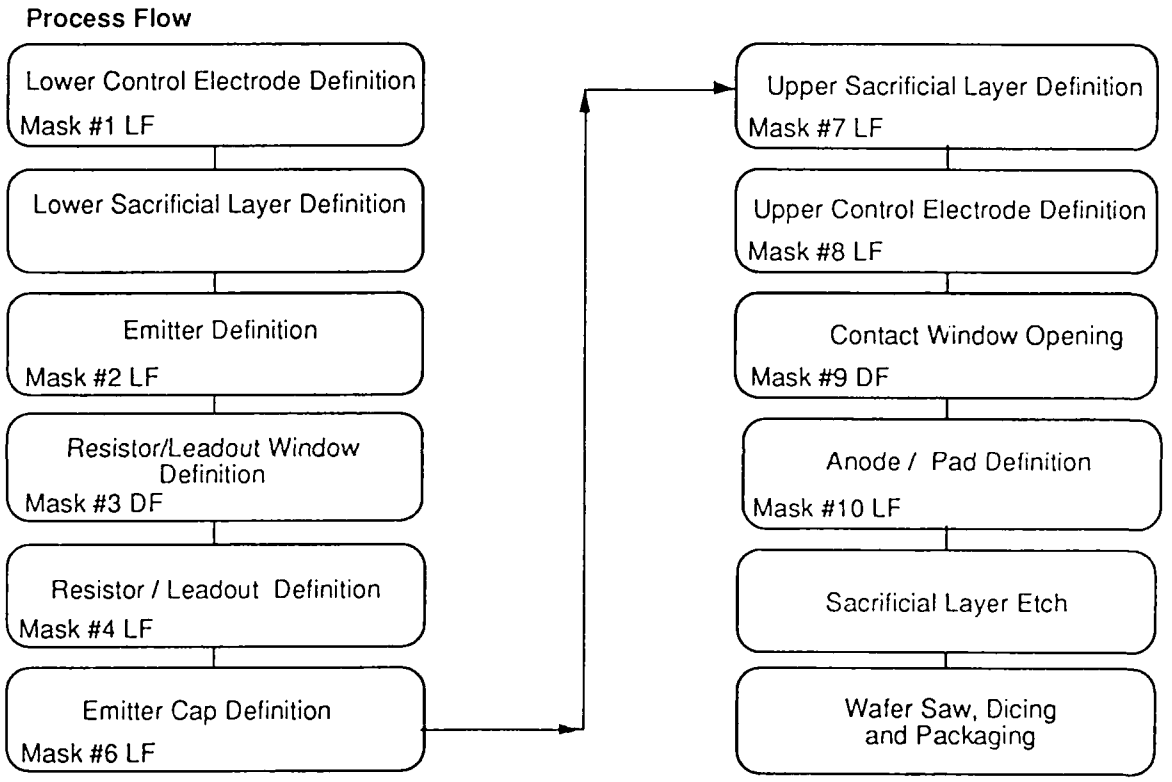


Figure 4.5. The Fabrication Process Flow.

The fabrication process is done on a Karl Suss contact aligner with an alignment tolerance of ±0.25 μm relative to the fiducials. The fabrication starts with the growth of 5 μm of oxide on a silicon wafer followed by the deposition of the lower gate (control electrode) layer. This layer consists of 1000 Å of silicon nitride and 1000 Å of TiW. Both layers are bias sputtered to produce very low stressed layers and, for the nitride, a layer that is resistant to BOE. The TiW layer is etched in a reactive ion-etcher in SF_6/He gas. This is followed by the deposition of about

3,500 Å of oxide in a PECVD reactor. The PECVD oxide is chosen as opposed to other oxides because of the relative ease of removal in BOE during sacrificial layer etch. This is followed by the deposition of a 1500 Å nitride layer that is bias sputtered. The nitride layer has the following properties (i) good step coverage (so that it covers the 1,000 Å TiW step), (ii) good etch resistance (for selectivity during the final sacrificial layer etch), and (iii) low stress (for cantilever beam or plate or free standing structure after the sacrificial layer deposition). This deposition is followed by the deposition of 300 - 400 Å of TiW (the emitter) with a protective coating of 500 Å of bias sputtered quartz (etch stop for the resistor definition). The emitter is defined by the second mask through a combination of C_2F_6/CHF_3 plasma for the oxide and SF_6/He RIE for the TiW. A contact window is opened in the oxide for the resistor layer with the third mask using BOE. The resistor layer is 1000 Å of TaN which is reactively sputtered in nitrogen. The sheet resistance of this layer is varied between 10 Ω/sq to 10^7 Ω/sq by changing the nitrogen concentration. The resistor layer is defined by SF_6/He RIE with the fourth mask. The oxide layer protects the emitter during this etch. After the resistor definition, the protective oxide layer is removed prior to the bias sputter deposition of the upper nitride cap layer. This layer is also 1500 Å thick and the stress has to be controlled to allow the emitter to be free-standing after the sacrificial layer oxide removal at the end of fabrication. The emitter cap is defined by the fifth mask. This etch defines the emitting edge and the support nitride layer. The upper nitride layer is etched in a C_2F_6/CHF_3 plasma followed by ion-mill of the 300 Å TiW emitter and, finally, the lower nitride layer is etched in a C_2F_6/CHF_3 plasma. The final etch also removes some of the lower sacrificial layer. The nitride layer becomes slightly recessed at this point because of the selectivity between the TiW and nitride in the C_2F_6/CHF_3 plasma. Figure 4.6 is an SEM of the structure after the emitter cap etch showing the emitter is exposed. The upper sacrificial layer, 3,500 Å of PECVD oxide, is then deposited and it is defined by the sixth mask. The upper and lower sacrificial layers are etched at that point to expose the lower gate (control electrode) for contact to the upper gate. The upper gate (control electrode) is then deposited. It consists of 2500 Å of TiW and 2500 Å of nitride. Both layers are bias sputtered to attain the following

characteristics: (i) step coverage (there are significant steps at this point ≈1μm) and (ii) low stress (so that free-standing films can be obtained after sacrificial layer etch). The upper gate (control electrode) is supported on the top side by a thick nitride layer because of the expected electrostatic forces on the upper gate when the device is biased. The layer is defined by nitride etch in C_2F_6/CHF_3 plasma and TiW etch in SF_6/He RIE. The contact window for the gate and emitter are next opened up after the deposition of a 7,500 Å oxide protective layer. This also opens up the anode region. The window is opened by a combination of BOE of oxide and C_2F_6/CHF_3 plasma etch of nitride. Finally, a 5000 Å of TiW is deposited and defined by SF_6 plasma etch after the ninth mask lithography. The total depth of the microstructures is, by this time, ≈2 μm. The sacrificial layers are removed by buffered HF solution.

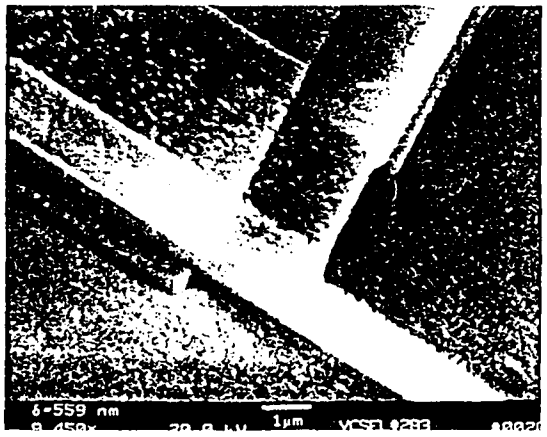


Figure 4.6. SEM of the Emitter after the definition of the Emitter Cap Layer. It shows that the emitter is exposed. The tilt angle was 75 °.

Figures 4.7 and 4.8 are SEMs of the microstructure before and after the removal of the sacrificial layer. It shows that the emitting edge is exposed as expected.

Device Evaluation

Figure 4.9 shows the test set up for the vacuum transistor. The vacuum was maintained at a pressure less than 1 x 10^{-8} torr. Two groups of devices were characterized.

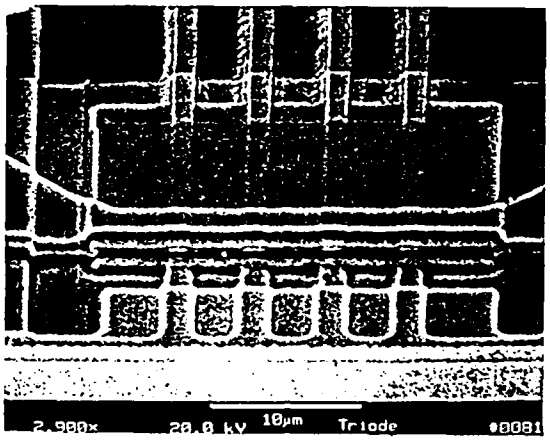


Figure 4.7. SEM of the microstructure after the removal of the sacrificial layer. It shows that the emitter segments.

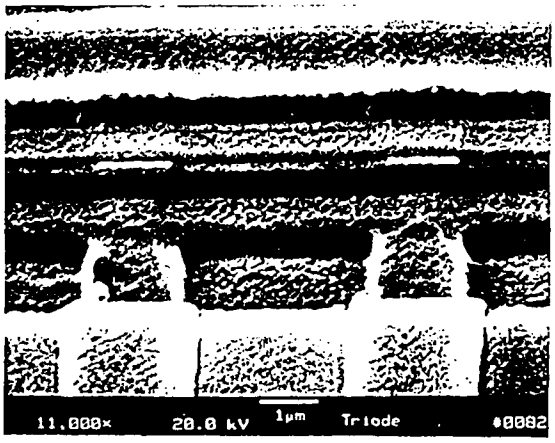


Figure 4.8. SEM of the microstructure after the removal of the sacrificial layer. It shows that the emitting edge is exposed as expected.

Device 1

The first group of devices (Device 1) have 400 Å TiW emitters and gate-to-emitter separation of 7,000 Å. The anode-to-emitter separation was 5 µm. Device 1 does not have on-chip resistors. Figure 4.10, 4.11, and 4.12 show the transfer characteristics, Fowler Nordheim plot and transconductance of a vacuum transistor that has 300 Å TiW emitter and 7000 Å gate-emitter separation. The anode voltage was 400 V and the devices do not have on-chip resistors for protection. The device turns on at 70 V and a gate voltage of 180 V. The emitted current is 2 µA.

The maximum transconductance of this device is 0.1 μS. The device follows the Fowler-Nordheim characteristics and the extracted values of a_{FN} and b_{FN} are 1.2 x10-8 and 946.6, respectively.

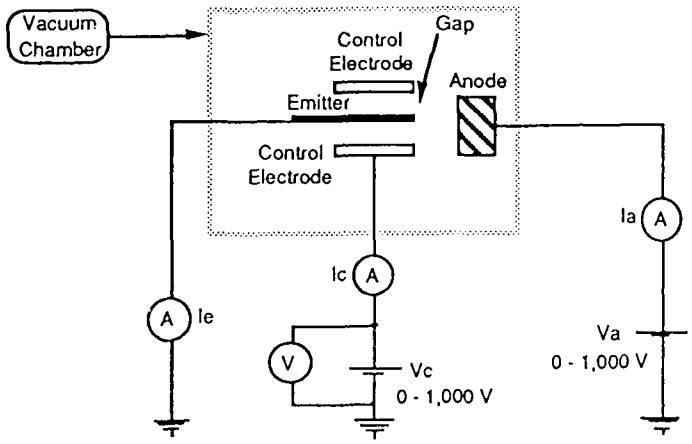


Figure 4.9. Test-Set Up for the Vacuum Transistor. The vacuum was maintained at < 1 x 10^{-8} torr.

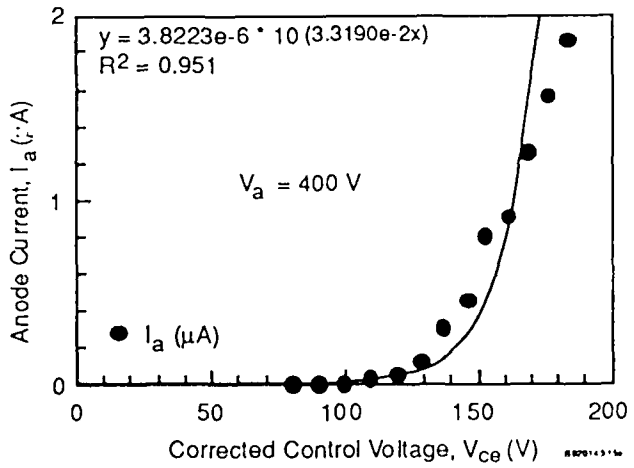


Figure 4.10. The Transfer Characteristics of a Vacuum Transistor (Device 1) that has 300 Å TiW Emitter and 7000 Å Gate-Emitter Separation. The anode voltage was 400 V and the devices do not have on-chip resistors for protection.

Device 2

The second group of devices (Device 2) have integrated on-chip resistors. Figure 4.13 and 4.14 are the output and transfer characteristics of a vacuum transistor that has on-chip TaN

resistors. The emitter is 300 Å TiW and the gate-emitter separation is 5,000 Å. We could not take the Fowler-Nordheim characteristics because of the on-chip resistors which are sometimes nonlinear. We observe from Figure 4.14 that the IV characteristics is triode-like. The anode-emitter separation is nominally 5 μm, but we found out from SEM analysis that there are protrusions formed in the anode that reduced the anode-emitter spacing to about 1 μm. The emitter current was exactly equal to the anode current while the gate current is negligible. Figure 4.15 shows on a time base the emitter anode and gate currents as the anode voltage is ramped up and later the gate voltage is ramped up. In the cases where a negative gate voltage is applied, we observe no emitter or anode currents. At very high negative biases, there is some leakage between the anode and the gate. It is interesting to observe that a gate voltage of 250 V and anode voltage of 200 V, we observe emission currents with 99% of the emitted current collected by the anode even though it is at lower voltage. This is an indication of the symmetry of the upper and lower gate electrodes around the emitter. Table 4.2 is a summary of the best emission data obtained from the wafer. We also performed low frequency modulation of the vacuum transistor as shown in Figure 4.16.

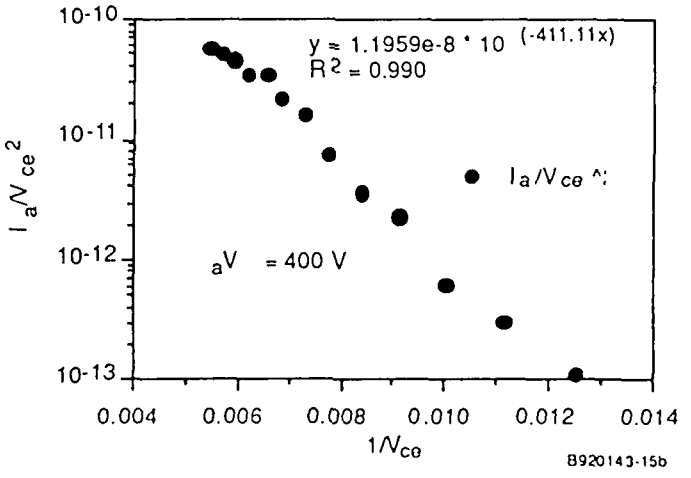


Figure 4.11. The Fowler-Nordheim Characteristics of a Vacuum Transistor (Device 1) that has 300 Å TiW Emitter and 7000 Å Gate-Emitter Separation. The anode voltage was 400 V and the devices do not have on-chip resistors for protection.

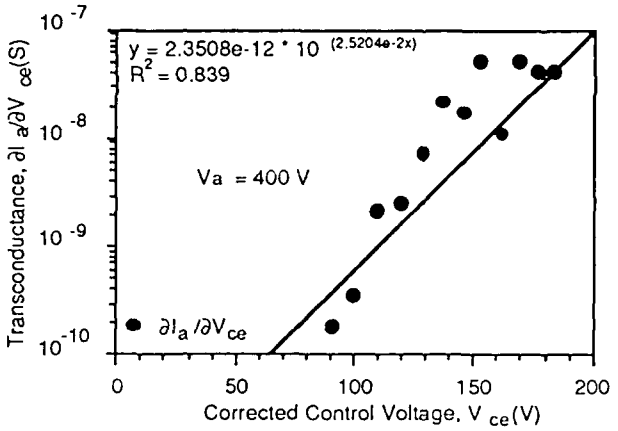


Figure 4.12. The Transconductance of a Vacuum Transistor (Device 1) that has 300 Å TiW Emitter and 7000 Å Gate-Emitter Separation. The anode voltage was 400 V and the devices do not have on-chip resistors for protection.

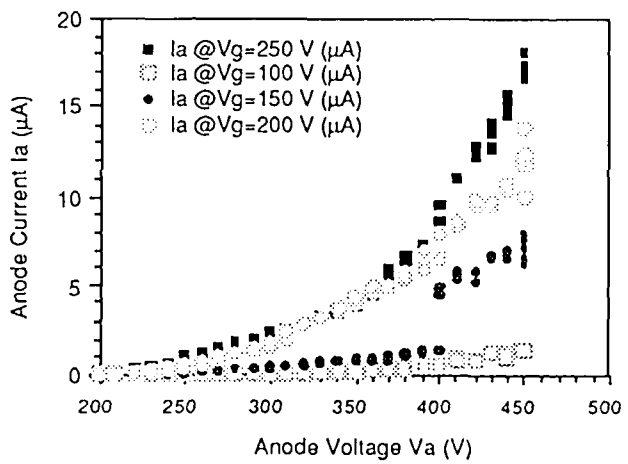


Figure 4.13. The Output Characteristics of a Vacuum Transistor that has on-chip TaN Resistors. The emitter is 300 Å TiW and the gate-emitter separation is 5,000 Å.

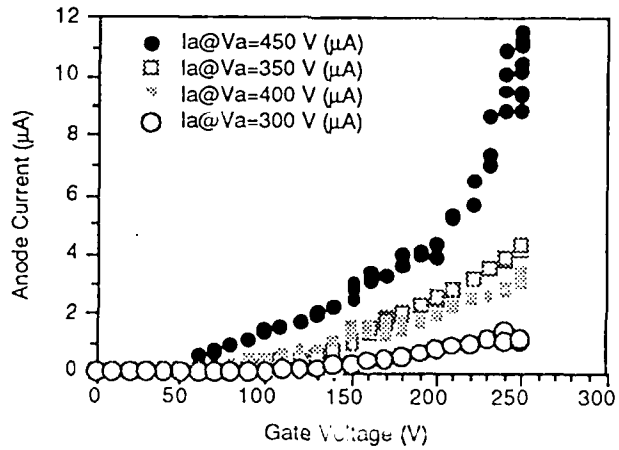


Figure 4.14. The Transfer Characteristics of a Vacuum Transistor that has on-chip TaN Resistors. The emitter is 300 Å TiW and the gate-emitter separation is 5,000 Å.

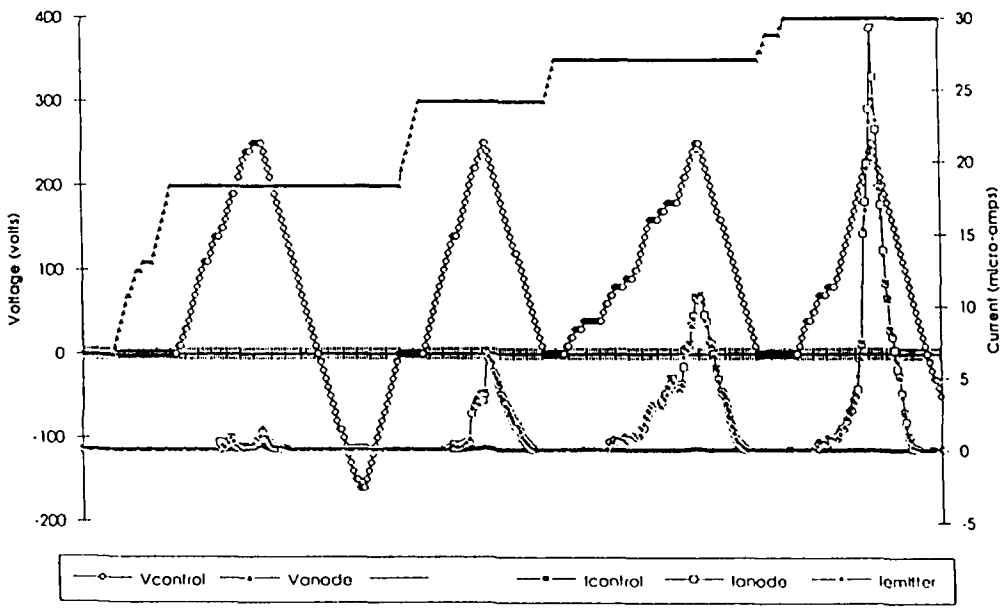


Figure 4.15. A Time Base the Emitter Anode and Gate Currents as the Anode Voltage is varied and later the Gate Voltage is varied.

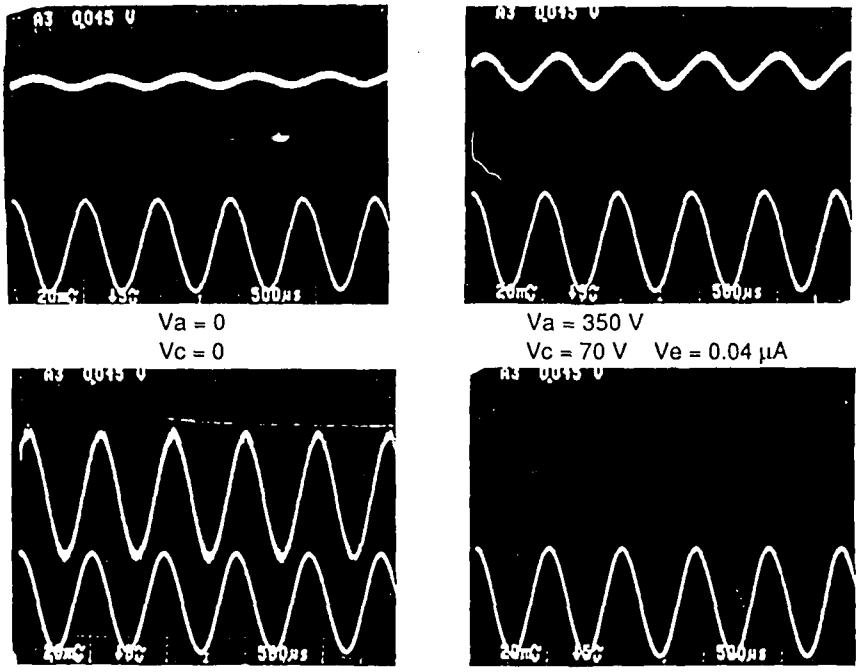


Figure 4.16. Low Frequency Modulation of the Thin-Film-Edge Emitter Vacuum Transistor.

Table 4.2. Summary of Device Results for Vacuum Transistors (Device 2)

Device Parameter	Measured Value
Device Width	4 μm
Turn-on Voltage (0.1 μA)	50 Volts
Max Current	50 μA
Current Density	12.5 μA / μm
Extrinsic Transconductance (including 1 MΩ resistor)	0.6 μS / μm
Intrinsic Transconductance (excluding Resistor)	1.5 μS / μm
Capacitance [2.5 μm gate length]	0.3 fFarad / μm
ft (calculated)	1.06 GHz
Emission Time (measured)	4 hours

Discussion

Based on the FN equation, we can obtain expressions for the emission area α and the field factor β with the experimentally measured quantities a_{FN} and b_{FN} as parameters [2].

$$\alpha = \frac{1.219\, a_{FN}\, b_{FN}^2}{A\, B^2\, \emptyset^2 \exp\left[\frac{1.44 \times 10^{-7}\, B}{\sqrt{\emptyset}}\right]}$$

$$\beta = \frac{0.95\, B\, \emptyset^{3/2}}{b_{FN}}$$

From Figure 4.11, we determined that $a_{FN} = 1.1959 \times 10^{-8}$, $b_{FN} = 946.6$. We do not know the exact value of Ø, but we can assume a value of 4.5 eV which is reasonable for W, then $\alpha = 8.37 \times 10^{-16}$ cm^{-2}, and $\beta = 6.58 \times 10^5$ cm^{-1}.

The emission area derived from the data is quite small. The corresponding current density, assuming the emission area is correct, is about 2.39×10^9 A cm^{-2}, which is quite high and well beyond the electromigration limit for most metals. We examined the sensitivity of the field factor β and emission area α to the assumed value of the work function Ø. Table 4.3 gives the value of α and β assuming Ø = 3.5 eV, 4.5 eV and 5.5 eV. The table shows that while β varies with Ø, α is almost insensitive to Ø because the quantity $f(\emptyset) = \emptyset^2 \exp\left[\frac{1.44 \times 10^{-7}\, B}{\sqrt{\emptyset}}\right]$ varies very little in the range $3.5 \le \emptyset \le 5.5$.

Table 4.3. Variation of the emission area α and the field factor β with the work function and the corresponding radius of curvature.

	Work Function		
Parameter	Ø = 3.5 eV	Ø = 4.5 eV	Ø = 5.5 eV
α	7.41×10^{-16} cm^{-2}	8.37×10^{-16} cm^{-2}	8.75×10^{-16} cm^{-2}
β (= 1/kr)	4.51×10^5 cm^{-1}	6.58×10^5 cm^{-1}	8.89×10^5 cm^{-1}
r (assume k=10)	2.22×10^{-7} cm	1.52×10^{-7} cm	1.12×10^{-7} cm
f(Ø)	2.43×10^3	2.15×10^3	2.06×10^3

The expected emission area for a perfectly smooth edge with an emission angle of $\pi/10$ would be π r L /10, where r is the radius of curvature (which in our case is half the thickness of the emitter) and L is the emitter width. In the above devices shown in Figure 4.11, L = 4 μm and

r is 150 Å giving an expected emission area of 1.89×10^{-10} cm^2 which is six order of magnitude higher than the emission area derived from the data.

If we assume that β is a function of the radius of curvature r, i. e. $\beta(r) \approx 1/kr$, where k is a function of both the emitter radius and the gate-to-emitter spacing. From our simulations, we confirmed that $8 \leq k \leq 15$ for a perfectly smooth edge emitter. Assuming that k is 10, the value of r will be 1.52×10^{-7} cm which is much smaller than the expected 1.5×10^{-6} cm. We expect that the emitter surface will not be perfectly smooth and we expect to have micro-protrusions on the surface since the film is either amorphous or polycrystalline because it was sputter deposited.

The experimental data for the second set of devices do show much higher current levels. We can not perform a similar analysis on the data because of the use of an on-chip series resistor. If we examine the low current regime, the emission current increases exponentially with voltage as expected, but it saturates at higher currents because of the resistor which was included to prevent burnout. The device results are encouraging because they indicate that the current levels can be much higher if the emitting edge is carefully cleaned. The devices show emission currents as high as 12.5 μA/μm of edge. While the devices are not yet at their optimal performance, the higher currents are indication that there are more emission sites on Device 2 than on Device 1. The results also confirm our speculation that the thin-film edge is a collection of closely packed points.

The above discussion and the data suggests that we are not obtaining uniform emission from the thin-film-edge emitter and that the emission is probably from one or two sites on the surface. This suggests that there is probably some oxide layer on the surface that is non-conducting and it is not allowing emission from a larger area. The above wafers have not undergone any special surface treatment such as UHV bake-out or hydrogen plasma cleans. Schwoebel et al [11] recently demonstrated improved performance from their FEAs after hydrogen plasma clean. Furthermore, Ti in the TiW films is known to oxidize easily. We use oxygen plasma at several stages in the process for removing photoresists. We believe that the surface oxides are preventing larger emission currents and that the devices will show much better performance once the surface

oxides are removed. We also expect much better performance if (i) a metal that does not form surface oxides such as W or Mo is used as the central emitter and (ii) if a lower work function metal is used as the central emitter.

Using the results tabulated in Table 4.2 and the equivalent circuit shown in Figure 4.17, we calculated the unity current gain cut-off frequency of this device to be about 1 GHz. The devices are obviously capable of much higher performance, but the number of emission sites has to increase. In order to attain higher performance device capable of microwave power amplification, the emitter performance has to be improved. The current density has to increase to about 50 μA/μm @ a gate voltage of 75 V and leading to a transconductance of 10 μS/μm of edge width @ a gate voltage of 75 V. The capacitance can be reduced to at 0.17 fF/μm by using control electrodes that are 2 μm long. This will lead to a device with a unity current gain cut-off frequency of ≈ 10 GHz. One distinct advantage of the device is the very small feedback capacitance between the gate and the anode. Using these initial results, we project that it should be possible to design and fabricate a device with 10 Hz and 10 W and 10 dB gain and a bandwidth of 3% if the performance of the emitter is improved by increasing the number of emission sites on the surface of the thin-film-edge.

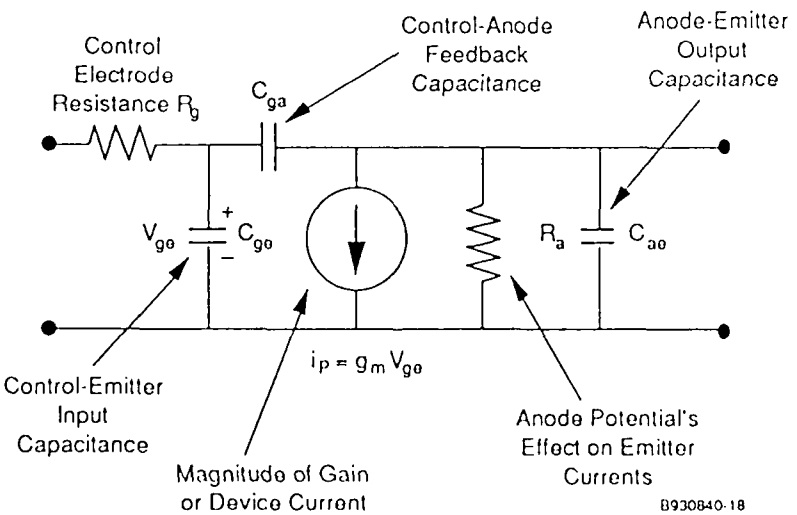


Figure 4.17. Equivalent Circuit of the Thin-Film-Edge Emitter Vacuum Transistor.

Summary

In this section, we report the design, fabrication, and evaluation of a thin-film-edge emitter vacuum transistor with current density of 12.5 μA/μm. Our analysis shows that the devices should be capable of much higher performance if the emission area increases by the removal of surface oxides. The results indicate the possibility of a new type of RF power source that will have the power handling capability of vacuum tubes and the batch fabrication and low-cost manufacturing of semiconductors. The device results confirm our speculation that the thin-film-edge emitter is a collection of closely packed emitting points, however, they all have to be activated by maintaining a very clean surface free of any oxides or contaminants.

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Section 5. Thin-Film-Edge Vacuum Transistor Amplifier

Based on the results of the vacuum transistor described in the previous section and on the analysis presented in Section 2, we concluded that a vacuum transistor array could be designed and configured for the purpose of demonstrating a microwave vacuum transistor amplifier for high-output-power density applications.

The technical issues that need to be addressed are related to the unity power gain cut-off frequency. As discussed in Section 2, f_{max} is related to both the unity current gain cut-off frequency, f_τ, and the device feedback elements between the input and the output

$$f_{max} \approx \frac{f_\tau}{2\sqrt{r_1 + f_\tau \tau}}$$

$$f_\tau \approx \frac{g_m}{2 \Pi Cin}$$

where g_m is the transconductance, Cin is the input capacitance, r_1 is the input-to-output resistance ratio, and τ is a time delay (constant)

$$r_1 = \frac{R_g + R_i + R_k}{R_p}$$

$$\tau = 2\Pi R_g C_{gp}$$

where R_g, R_I, R_k, R_p, and C_{gp} are defined in Figure 5.1, the simplified equivalent circuit of the vacuum transistor.

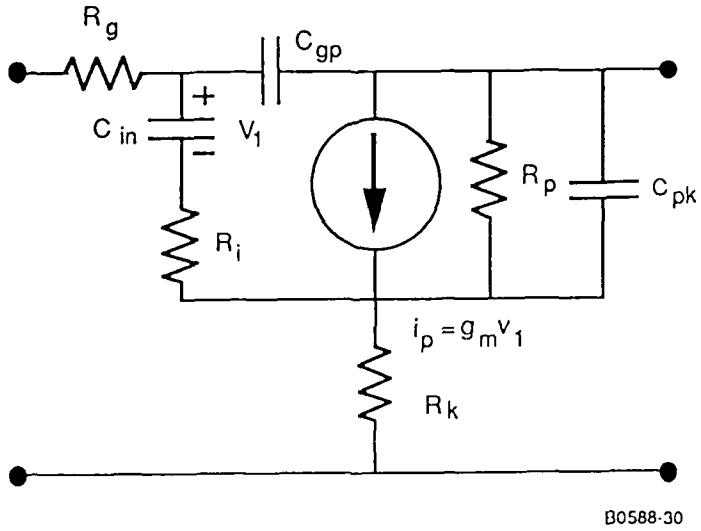

Figure 5.1. Simplified equivalent circuit used in design of the vacuum transistor amplifier.

The transconductance is given by

$$g_m = \frac{I}{V}\left[2 + \frac{b_{FN}}{V}\right]$$

The power gain, Gp, for a matched load is

$$Gp = \frac{Pout}{Pin} = \frac{Io^2RL}{\frac{Vin^2}{Rin}} = \frac{1}{4}\,gm^2 \bullet Rin \bullet RL$$

Thus, our technical approach to obtaining high f_{max} and f_τ has been to

- maximize current and current density
- maximize transconductance
- minimize the excitation voltage
- minimize gate capacitance
- minimize the feedback capacitance.

These were the factors taken into consideration in the design of the vacuum transistor array.

5.1 Vacuum Transistor Array Design

The vacuum transistor array design is based on the results of the previous section on TFEE vacuum transistors, shown in Table 5.1. This design is to demonstrate high current densities on vacuum transistors and modulation of the devices on wafer at 1 GHz. The vacuum transistor design goal is shown in Table 5.2 using the device parameters measured and shown in Table 5.1.

Table 5.1. Summary of vacuum transistor device results.

Device Parameter	Measured Value
Device width (gate length)	4 μm
Turn-on voltage (0.1 μA)	50 V
Maximum current	50 μA
Current density	12.5 μA/μm
Extrinsic transconductance (including 1MΩ resistor)	0.6 μS/μm
Intrinsic transcondlucatnce (excluding resistor)	1.5 μS/μm
Capacitance	0.3 fF/μm
f_τ (calculated)	1.06 GHz
Emission time (measured)	4 hr

Table 5.2. Microwave vacuum transistor design goals.

Device Parameter	Device Value
Control electrode length	2 μm
Emitter current density	10 μA/μm
Transconductance	1.7 μS/μm
Input capacitance	0.17 fF/μm
Current gain cutoff frequency	1.58 GHz
Maximum available gain at 1 GHz	9.5 cB

The devices were designed to have width of 2,400 μm. Assuming a current density of 10 μA/μm, this gives an expected emission current of 24 mA. This current is more than adequate for demonstrating modulation at 1 GHz on wafer. The emitters are divided into 12 segments or stripes, each 200 μm long. Each emitter segment has two gates—one above and one below; and an anode. The emitter segments are connected in parallel and are all tied to the ground. The gate

segments are connected in parallel and are tied to the input pad. The anode segments are all tied in parallel and are all tied to the output pad.

Each emitter segment is subdivided into smaller vacuum transistor building blocks. These building blocks have emitter edge widths of 3 μm to 200 μm. Figure 5.1-1 shows the top view of a device with emitter building block width of 50 μm. There are 12 segments each containing four building blocks. The microwave transistor has pad metalization that makes the device probable on wafer and can be tested at frequencies up to 2 GHz. The input (gate) and output (anode) pads are both surrounded by ground planes (emitter) on either side. The arrangement is very similar to devices that are designed to be probed by cascade microprobes. Figure 3 shows the top view of one of the devices. Details of device layout are given in the attached mask documentation.

The devices were designed with device parameters shown in Table 5.1 using the equivalent circuit shown in Figures 5.1-2(a) and (b). The device has 2,400-μm-wide emitter with a current of 24 mA, a transconductance of 3.6 mS, and a capacitance of 408 fF (including pads and crossovers). This leads to a unity current cutoff frequency of 1.58 GHz and a maximum available gain of 9.5 dB at 1 GHz.

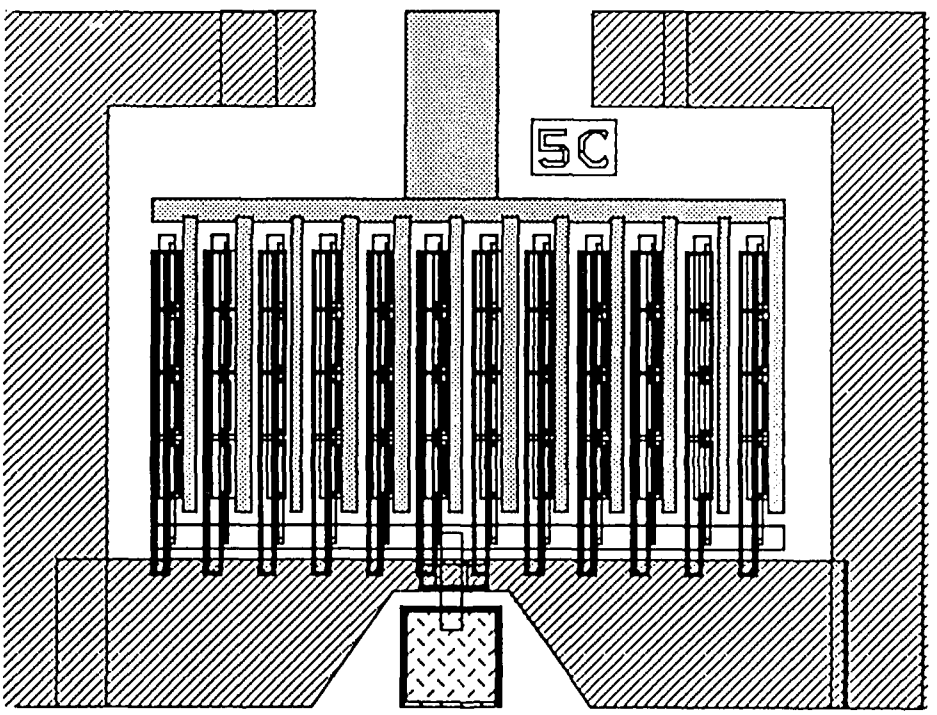

Figure 5.1-1. Microwave vacuum transistor device layout.

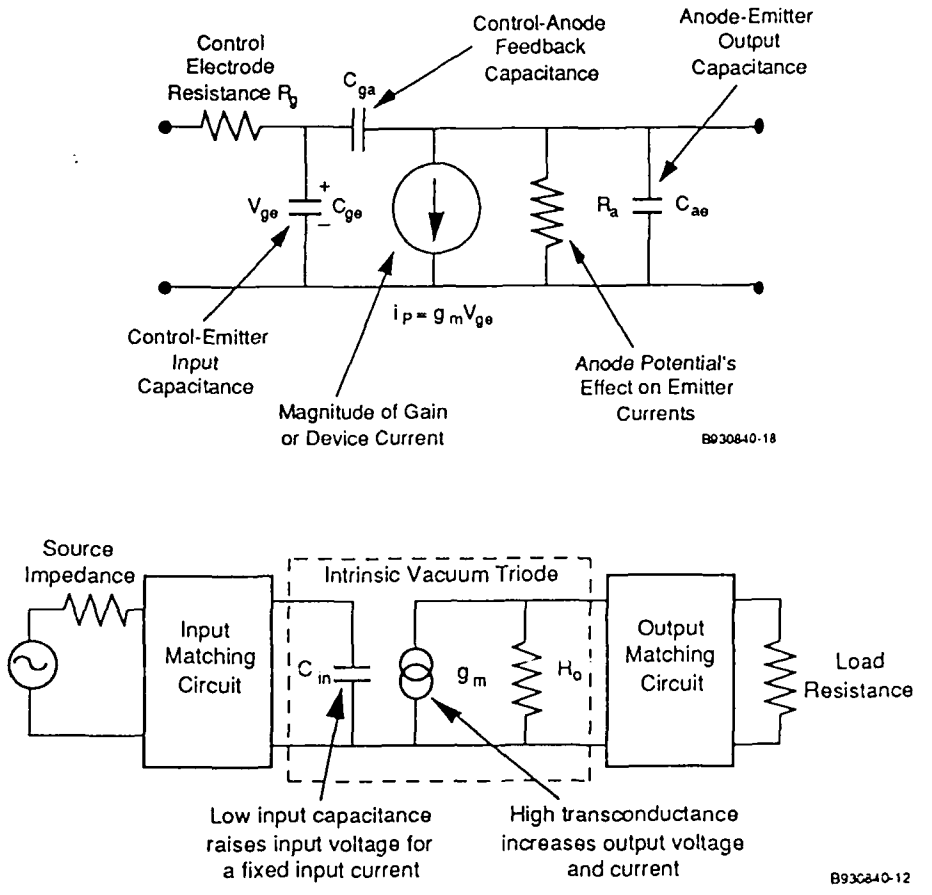

Figure 5.1-2. Schematic diagram of the thin-film-edge emitter vacuum transistor equivalent circuit.

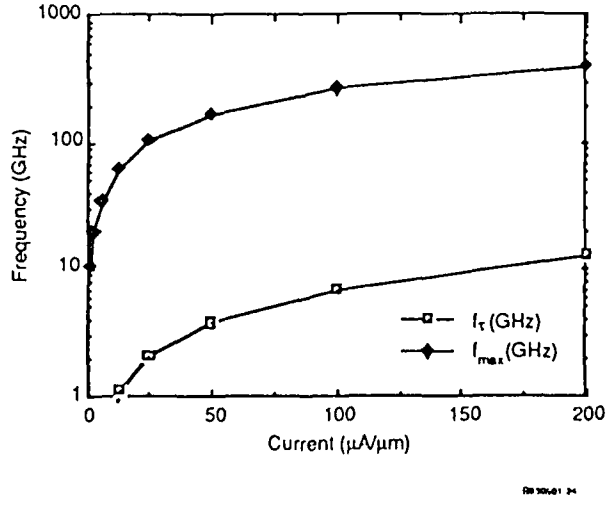

Figure 5.1-3. Calculated f_τ and f_{max} of the microwave vacuum transistor.

Figure 5.1-3 shows the calculated f_t and f_{max} of the device as a function of the current density. It shows an f_τ of 1 GHz and f_{max} of 30 GHz at current density of 10 μA/μm. It also shows further performance improvement if the current density is increased to 25 μA/μm or 50 μA/μm.

5.2 Process Development

The process for the fabrication of thin-film-edge emitter vacuum transistors and vacuum transistor arrays requires the precision of IC and micromachining technologies. We made a number of significant advances and improvements during the program. There is no doubt that the fabrication process is at the cutting edge of both IC and surface micromachining technologies. The advances and improvement include:

- Fabricating a thin-film edge with good step coverage over existing lower gate metalization
- Thin-film resistor process (10 - 10^7 Ω/sq.)
- Symmetrically layered gates about a central thin-film-emitter
- Stress-free and free-standing thin-film-edge emitter supported by nitride layers
- Selective sacrificial layer etches
- Lithography with ± 0.1 μm tolerance
- Lithography over layers with 2 μm depth of field
- Alignment of lower gate-to-emitter-to-upper gate
- Free-standing, stress-free upper gate
- Step coverage of anode fingers from elevated area into wells
- Selective and anisotropic etches of resistor, emitter metal, and gate metal layers.

These were all serious challenges that were not anticipated in the program, but needed to be solved to demonstrate the vacuum transistor array.

5.3 Vacuum Transistor Array Fabrication

The vacuum transistor array process is very similar to the vacuum transistor process. However, there are minor but significant differences. The lithography system was changed from

a contact aligner to a 10:1 stepper projection aligner. This is because the device is much bigger and it is important to have precise alignment of the lower gate, emitter, and upper gate. Secondly, the projection aligner is much cleaner because there is no contact between the mask and the wafer. This reduces the defect density significantly. There were a number of process development issues that resulted in the loss of three runs; however, the fourth run was successful. Figure 5.3-1 shows the process flow.

Figure 5.3-2 shows a vacuum transistor array amplifier/device indicating the emitter, gate, and anode. Figures 5.3-3 and 5.3-4 are close up views showing the emitter/gate structure and the emitting edge, respectively. Figure 5.3-4 shows the 300Å emitter is surrounded by two nitride layers, each 1,500Å thick.

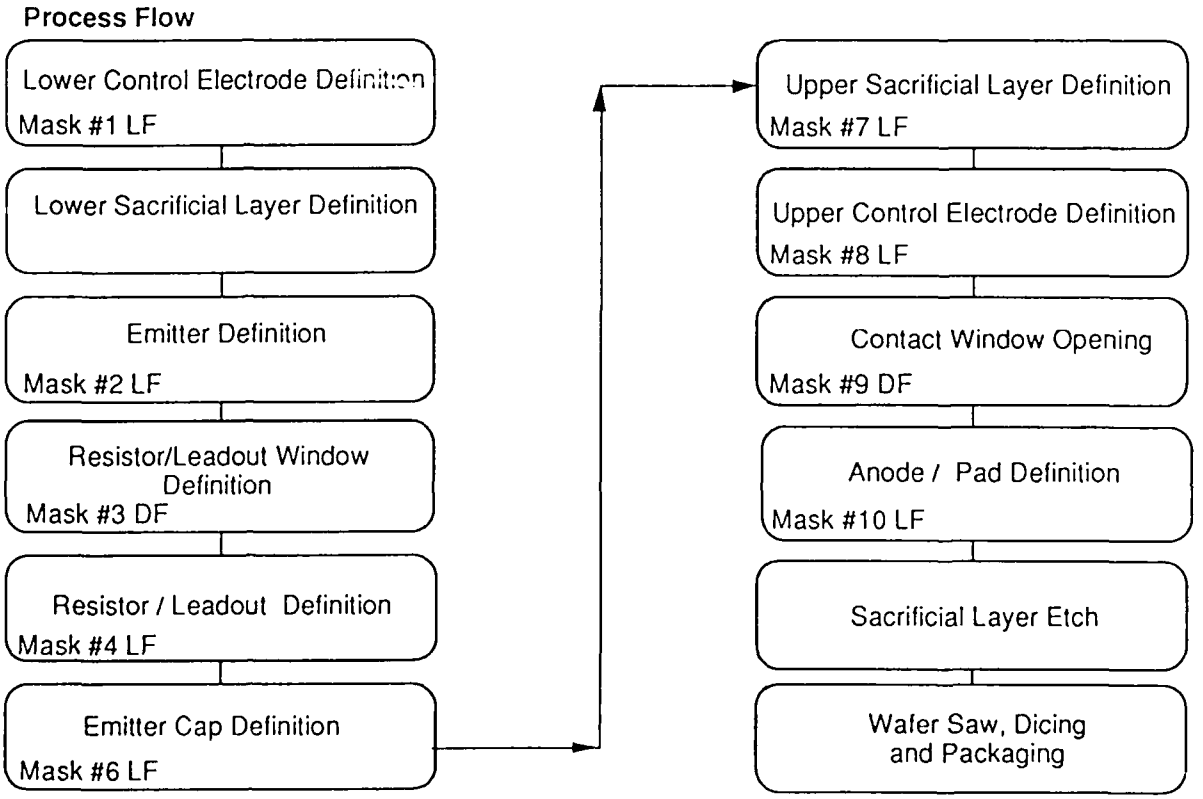

Figure 5.3-1. Fabrication process flow for the microwave vacuum transistor.

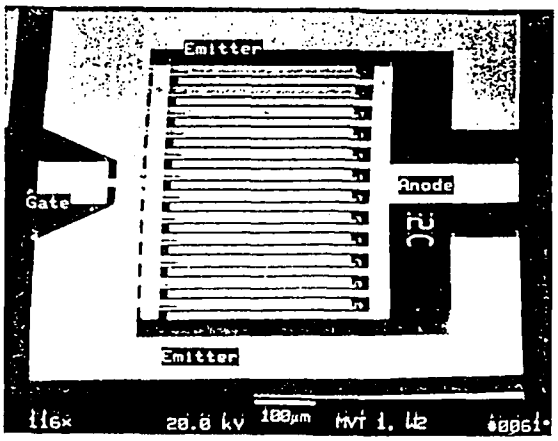

Figure 5.3-2. SEM of the vacuum transistor amplifier.

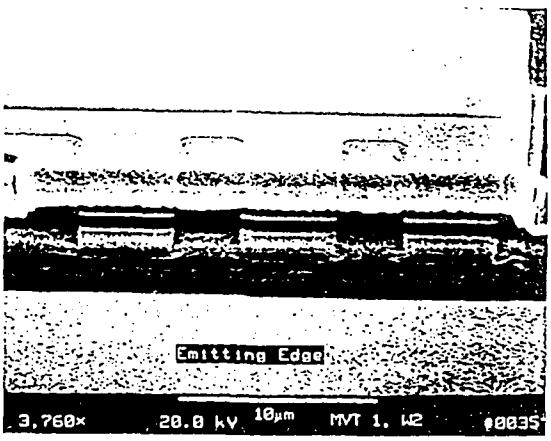

Figure 5.3-3. SEM of the emitter/gate structure of vacuum transistor amplifier.

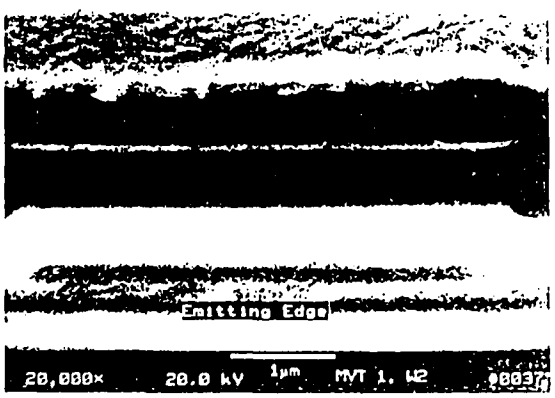

Figure 5.3-4. SEM of the emitting edge of microwave vacuum transistor.

The sacrificial oxide layer was removed by patterning the wafer to expose only the region between the anode and the gate. The oxide was removed using a combination of dry etch in (C_2F_6/CHF_3 plasma) and a wet etch (BOE). The resist was removed using a combination of wet chemistry (PRS 1000) and dry ash (O_2 plasma).

5.4 Vacuum Transistor Array Evaluation

Our initial characterization of the vacuum transistor arrays indicate the current densities are not as high as we expected. We measured currents of less than 50 μA, which indicates only a single point is emitting electrons. We believe that the surface of the emitter is covered with an oxide preventing electron emission. This oxide has to be removed to obtain large scale emission of electrons.

We are developing approaches to remove the oxide layer with wet etches outside the vacuum. This will be followed by a hydrogen plasma after the wafers are loaded into vacuum.

Section 6. Conclusions and Recommendations

6.1 Conclusions

The RF Vacuum Microelectronics program successfully demonstrated the thin-film-edge emitter vacuum transistor. The technology promises to be the next advance in miniaturization of RF sources because it combines the advantages of solid-state microfabrication technology with those of electron transport in vacuum, giving the system designer, new system capabilities such as increased power density, increased efficiency, reduced temperature sensitivity, and radiation hardness. We predict that it should be possible to design a vacuum transistor amplifier capable of generating 10 W of power at a frequency of 10 GHz with 10 dB gain and in instantaneous bandwidth of 3%. However, there are several issues that we encountered during the course of this program. These issues must be resolved before the technology can attain very high performance. Some recommendations of how to achieve high performance are given in subsection 6.2.

The accomplishments of the RF Vacuum Microelectronics program are

Vacuum Diode

- Demonstrated high emission current from a single edge ($\simeq$ 400 μA)
- Demonstrated high emission current density from an edge ($\simeq$ 10 μA/μm)
- Demonstrated high emission current from a comb structure with current equalization resistors without burnout
- Demonstrated long-term device operation (>72 hours) at a high current level (50 μA)
- Performed a study of various emitter materials (TiW, WSi_x, Pt, WN_x, Mo)
- Demonstrated that the turn-on voltage can be reduced with Cs implants (from $\simeq$ 100 V to $\simeq$ 50 V)
- Demonstrated that Cs-implanted edge emitters can operate at high current densities (10 μA/μm). Operated a Cs-implanted edge emitter for ≥80 hours at 1 μA/μm.

Vacuum Transistor

- We have demonstrated a thin-film emitter vacuum transistor with symmetrically layered gate/control electrodes and integrated anodes
- The vacuum transistors have high currents (50 μA) and high current densities (10 μA/μm) and transconductance ≥1.5 μS. These values are above those considered necessary for 1 GHz operation.
- The devices have turn-on voltage as low as 50 V
- The devices have comb emitter structures with integrated resistors and capacitors on chip
- The devices have high-, short-, and long-range uniformity suggesting that large arrays of vacuum transistors can be connected in parallel to fabricate high-current and high-gain devices
- The devices have very low capacitances
- We have demonstrated all device and fabrication requirements necessary for 1 GHz operation of vacuum transistors with gain.

Process Development and Device Modeling

- Developed a thin-film resistor process with sheet resistances ranging from 1 Ω/sq to 10^7 Ω/sq for current equalization of vacuum transistors
- Developed silicon dioxide and silicon nitride processes for sacrificial layers and support layers resulting in mechanically robust vacuum transistors
- Developed processes for smooth thin-film-edge emitter that will result in smaller radius of curvature and higher currents and transconductance and higher frequency operation of the vacuum transistor
- Performed mechanical modeling and determined optimum vacuum transistor structure
- Performed electrostatic simulation for the determination of optimum emitter structure and the placement of the control electrodes. This resulted in a more robust vacuum transistor.
- Performed thermal modeling of the vacuum transistor to determine burnout mechanisms. This will have implications for future designs and post-fabrication processing.

- Performed a microwave analysis of the vacuum transistor to determine the optimum device parameters and device structure.

Device Modulation at 1 GHz

We did not demonstrate 1 GHz modulation, even though all device parameters such as current density, transconductance, and capacitance all indicate that 1 GHz modulation should be possible. We attribute the lack of modulation to the following reasons:

- Our test setup uses on-wafer probing techniques which introduces a lot of parasitic capacitances. It, thus, requires a minimum current of 20 mA to drive the probes or a gain of at least -50 dB.
- Our devices have very low total current even though we have demonstrated large current densities on narrower devices. This is because the total current does not scale with width because of non-uniform emission.
- The emission currents are small and the total emission area calculated from our analysis is only 10-5 of the total potential emitting area.
- We believe that the emitting area is covered with oxides and the current variation observed is consistent with a very small emission area varying from device to device.
- The oxides can be removed by wet chemical cleans prior to loading into vacuum followed by in-situ plasma. With the above recommended action, the total emission current should increase. We should be able to demonstrate 1 GHz modulation after these actions.

6.2 Recommendations

Although there has been a lot of progress made in the research and development of thin-film-edge emitter vacuum transistors as the basis for future RF sources, there remains a number of critical issues that need to be addressed before the successful demonstration of the vacuum transistor amplifier and its successful application into systems.

Our recommendations for these issues are:

- Development of approaches to prevent emitter burnout
- Development of approaches to obtain uniform emission

- Development of simpler fabrication process for the vacuum transistor microstructure
- Development of a thermal management approach
- Development of approaches to self-align the emitter and the gates
- Development of approaches for simpler sacrificial layer etch.

These recommendations are based on our results and our analysis of the requirements to build an RF vacuum transistor capable of generating 10 W of power at a frequency of 10 GHz with a gain of 10 dB and an instantaneous bandwidth of 3%. The results and requirements are shown in Table 6.2-1.

We recommend that research and development efforts should be expanded to include new applications such as flat panel displays and sensors. These efforts should place a strong emphasis on understanding the basic physics and fundamental mechanisms of 3D nanostructures, device operation, and device failure.

Table 6.2-1. Device Requirements for 10 GHz, 10 W, 10 dB Thin-Film-Edge Microwave Vacuum Transistor Amplifier.

Device Parameter	Current Status	Amplifier Requirements	Technical Approach
Device width	4 μm	3.2 cm	Layout wider device
Operating current	50 μA	320 mA	Increase device width
Turn-on voltage	50 V	20 V	Emitters with small radius of curvature (75 Å) and low-work-function material (≤2.5 eV)
Operating gate voltage	200 V	75 V	Same as above
Current density	12.5 μA	10 μA	Same as above
Transconductance	1.5 μS/μm	2 μS/μm	Same as above
Capacitance	0.3 fF/μm	0.08 fF/μm	Decrease gate length from 4 to 1 μm
f_τ	1.1 GHz (calculated)	4 GHz	Increase transconductance and decrease capacitance
f_{max}		20 GHz	Same as above